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Design and analysis of low-power high-speed shared charge reset technique based dynamic latch comparator

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ABSTRACT

Circuit intricacy, high-speed, low-power, small area requirement, and high resolution are crucial factors for high-speed and low-power applications like analog-to-digital converters (ADCs). The delay analysis of classical dynamic latch comparators is presented to add more insight of their design parameters, which effects the performance parameter. In this research, a new architecture of dynamic latch comparator is presented, which is able to provide high-speed, consumes low-power and requires smaller die area. The proposed comparator benefits from a new shared charge logic based reset technique to achieve high-speed with low-power consumption. It is shown by simulation and analysis that the delay time is significantly reduced compared to a conventional dynamic latched comparator. The proposed circuit is designed and simulated in 90 nm CMOS technology. The results show that, for the proposed comparator, the delay is 51.7 ps and consumes only 33.62 μW power, at 1 V supply voltage and 1 GHz clock frequency. In addition, the proposed dynamic latch comparator has a layout size of 7.2μm × 8.1μm.

1. Introduction

Data converters, i.e. Analog-to-digital converters (ADC) have become a constituent component which drives the semiconductor industry over the past few years. More and more functional blocks are integrated within a single chip, making this component more conventional and they are able to provide high-speed with low-power dissipation. In addition to these, as most of the devices are becoming portable and battery operated, the features of ADCs like high-speed, low-power, and smaller area on die, make them widely acceptable to the semiconductor industry. All these concerns apply to the most usable representative of the ADCs: the comparator. However, transistor dimension scaling is not straightforward, as it requires gate-induced drain leakage, high channel doping, and band to band tunneling across the junction. Moreover, analog circuit design happens to be more complex to carry out the necessity of reliability, where supply voltages need to be decreased according to the small dimensions of the transistors [1,2]. In ultra-deep sub-micron CMOS technology, the threshold voltage of devices are also not scaled down at the same rate as the technology, which in turn makes comparator design more difficult and challenging at low supply voltage [1–3]. To compensate the reduction in the supply voltage, larger size transistors are used in the design, which in turn increases the power consumption and die size. Another problem in low supply voltage design is switching and input common-mode voltage range. In the literature, various techniques are reported to handle the low voltage design challenges, such as supply boosting technique [4,5], design using body-driven transistors [6,7], current-mode design [8], and using dual-oxide processes. Problem with body driven technique [6] is that, the transistor suffers from low transconductance as its counterpart (i.e. gate driven), it also adds more complexity in the design and fabrication process. For handling low voltage, not only technological advancement, but new circuit architectures can also be developed without adding more complexity in the circuit, to handle such issues in deep sub-micron technology.

Several architectures of high-speed comparators exist, such as the multistage open-loop comparator, the preamplifier latch comparator, and the regenerative latch comparator [1–3]. Among the different structures, high resolution and high speed can be obtained easily by using the multistage open-loop comparator. On the other hand, the latch-type comparator is the most usable clocked regenerative comparators due to its high-speed and low-power consumption. It is based on cross-coupled inverters latch. Latch-type comparators are able to accomplish decisions more rapidly with strong positive feedback and no static power indulgence. In Ref. [9], the author has presented the basic dynamic comparator and two new dynamic comparators, which are based on architectural modification for low-power and high-speed operation. Conventional single tail current dynamic latch comparator is presented in Ref. [10]. In

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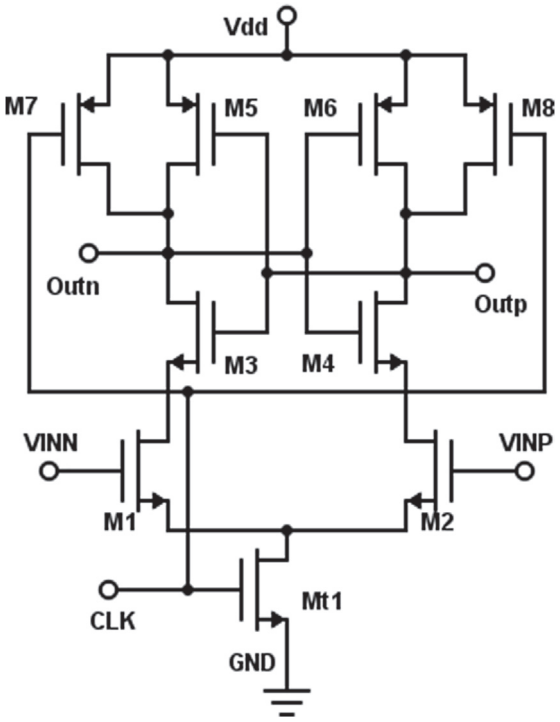

Fig. 1. Single tail current dynamic latch comparator.

Refs. [11,12], the author has presented unique reset technique for the dynamic latch comparator to reduce the delay and power named as shared charge logic. The first double-tail current dynamic comparator proposed in Refs. [13,14] is based on the architectural modification. In this, the author has modified the conventional single tail current dynamic latch comparator in to double tail current latch comparator, where the input and latch stages are separated to operate comparator with lower supply. The architecture level modification to improve speed of the comparator in low supply voltage is also reported in Ref. [15]. In this paper, author has modified the structure of latch into double cross-coupled latch to improve the speed of the dynamic comparator. The broad analysis about the delay of dynamic comparator is presented in Refs. [14–17]. By adding few minimum sized transistors to the conventional double tail current comparator, new dynamic comparators are proposed in Refs. [14–16]. Adaptive power control (APC) technique is reported in Ref. [18], for reduction in the power consumption.

This paper presents detailed analysis of different comparator architecture in terms of delay of dynamic comparator. This paper also discuss the reset schemes of conventional dynamic latch comparator. Based on the concept of shared charge in the reset phase, a new dynamic latch comparator is proposed, which does not require stacking of too many transistors or boosted voltage and can work at low supply voltage. The latch time and ultimately overall delay time is reduced by applying the shared charge logic based reset technique to the double tail current dynamic comparator. As a result of this modification, there is improvement in power and power delay product (PDP) as compared to referred comparators (viz. conventional single tail current, double tail current, modified double tail current and double tail current without inverted clock dynamic latch comparators).

The rest of this paper is organized as follows. The brief functionality and analytical expression of the single tail current dynamic latch comparator and double tail current dynamic latch comparator are presented in section 2. Each of this structure is discussed along with its advantages and disadvantages. Section 3 discusses the reset technique for dynamic latch comparator. Proposed comparator which is based on the shared charge logic based reset technique is discussed and analyzed in this section. Simulation results are presented in section 4, followed by concluding remarks in section 5.

2. Dynamic latched comparators

The strong positive feedback based dynamic latch comparators are preferable as compared to other architectures as they fulfils the requirements of high-speed and low-power ADC. Various performance parameters are analyzed and presented in literature, like noise [19], input referred offset voltage [20–22], kick-back noise [23], and random decision errors [24]. This section presents a comprehensive analysis of delay time for two commonly used topologies (i.e. single tail current dynamic latch comparator (STDLC) and double tail current dynamic latched comparator (DTDLC)) along with their merits and demerits.

2.1. Single tail current dynamic latched comparator (STDLC)

The schematic diagram of a single tail current latched comparator [2,9,10,13,16,25] is illustrated in Fig. 1. The operation of the comparator is divided in two phases: Reset phase (when CLK is low) and regeneration phase (when CLK is high). In the reset phase, M7 and M8 are ON, pulling the output terminals (Outn and Outp) to V_{dd}. Moreover, the tail current source, Mt1 is OFF, which eliminates the static currents from V_{dd} to ground (except the leakage currents which is negligible). In the regeneration phase, the current supply turns ON and the output voltages start to discharge to the ground with different discharging rate, proportional to their corresponding input voltages. The discharge will continue until the gate-source voltage of transistor M5 or M6 reaches under the threshold voltage of M5 or M6 and one of them turns ON. Subsequently, the latch (formed by transistors M3–M6) starts regeneration and forces one output to reach V_{dd} and the other one to the ground.

The transient behavior of the STDLC is depicted in Fig. 2. As shown in Fig. 2, the delay time is divided into two parts t_0 (time for discharging of load capacitance C_L, up to either of M5 or M6 turned ON) and t_{latch} (latch regeneration time). Assuming $V_{INP} > V_{INN}$, the M2 causes faster discharge of output terminal Outp and the t_0 can be found as follows:

$$t_0 = \frac{C_L \cdot |V_{thp}|}{I_2} \cong 2 \cdot \frac{C_L \cdot |V_{thp}|}{I_{t1}}, \quad \left(I_2 \cong \frac{I_{t1}}{2}, for\ small\ value\ of\ \Delta V_{diff} \right) \tag{1}$$

The latch regeneration time is calculated as per equation (2) [1,13]. It is assumed that the comparator is followed by the SR latch which enhances the output to full rail voltage [10] and hence half of the supply voltage is considered to be the threshold voltage ($\Delta V_{out} = V_{dd}/2$).

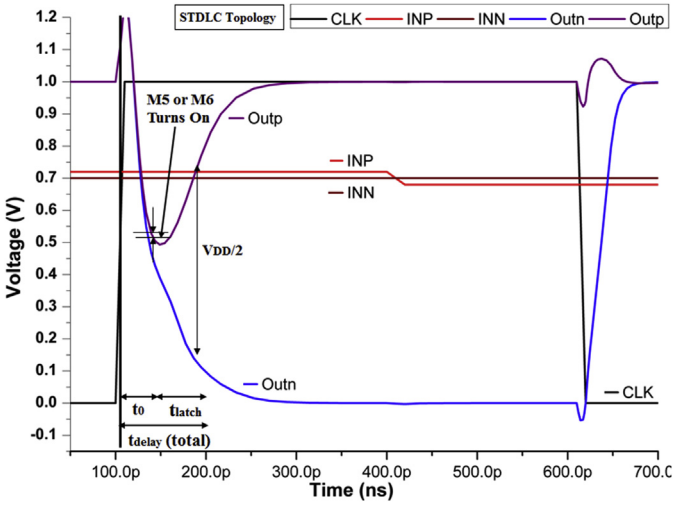

Fig. 2. Transient behavior of the single tail current based dynamic latched comparator topology with $V_{diff} = 20$ mV, $V_{cm} = 0.7$ V, $V_{dd} = 1$ V, and CLK = 1 GHz.