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Energy-efficient magnetic 4-2 compressor

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A B S T R A C T

In this paper, we present a hybrid MTJ/CMOS based low-power design of a 4-2 compressor. Furthermore, to gain more energy efficiency we implemented the proposed design with carbon nanotube field effect transistor (CNFET) technology and compared it with the MTJ/CMOS design. Simulations are performed at 45 nm and 32 nm CMOS technology with perpendicular anisotropy CoFeB/MgO MTJ model using Cadence Spectre simulator. Simulation results indicate that our hybrid MTJ/CMOS-based design has about two times lower power-delay product compared to the previous CMOS-based designs. Also, our MTJ/CNFET compressor has more than 3.5 times lower PDP compared to the CMOS based design.

1. Introduction

Multipliers are one of the most significant blocks in the design of digital signal processors, microprocessors and digital filters. Multipliers play an important role in digital signal processing, digital image processing and various other applications [1]. In general, the multiplier architecture consists of a partial product generation stage and partial product reduction stage to give the final binary result. The summation of partial products in the multiplier design contributes to most of the delay and area of the multiplier. Therefore, to reduce the accumulation of partial products in multiplier design, compressor circuits are used.

In digital circuits, the power consumption and speed are considered as the critical parameters in the design. Various methods have been proposed for designing low power circuits in the literature [2–4]. One approach for designing low-power circuits is to employ non-silicon based devices and nano-emerging technologies such as quantum dot cellular automata (QCA) [5], carbon nanotube field effect transistor (CNFET) [6], spin based devices [7], etc. Among these new technologies, spin based devices have attracted attention because of their promising characteristics such as near-zero standby power, non-volatility, high integration density, etc. [8,9].

Furthermore, a Logic-in-memory (LIM) paradigm can realize ultra-low-power architectures where memory elements are distributed over logic circuits [10,11]. Further, LIM can reduce the delay of circuits by minimizing the long interconnection wires. Also, RAM based circuits have zero static power dissipation and they are very appropriate to achieve high performance and low-power designs [12]. Magnetic Tunnel Junction (MTJ) is a spin based device which is most suited to use in LIM architectures because of its short access time, small dimensions and compatibility with CMOS technology, etc. [7,11,13–15].

In recent years, various hybrid MTJ/CMOS logic and arithmetic circuits such as magnetic full adder cell (MFA), magnetic flip-flop (MFF), magnetic look-up-table (MLUT) and magnetic content addressable memory (MCAM) have been proposed [11,16–19]. To the best of our knowledge, this is the first work to design 4-2 compressor circuit using hybrid MTJ/CMOS circuits.

In this paper, we present a hybrid MTJ/CMOS based low-power design of a 4-2 compressor. The proposed hybrid MTJ/CMOS compressor is simulated and compared with the existing CMOS designs using Cadence Spectre simulator. The proposed 4-2 compressor using hybrid MTJ/CMOS circuits has been evaluated using 45 nm standard CMOS technology along with the MTJ device [20–22]. Further, process, voltage and temperature variation of the proposed design has been performed and compared with the existing designs of 4-2 compressors. Also, the proposed design has been implemented with CNFET technology with MTJ devices and compared with the 4-2 compressor design implemented using MTJ/CMOS design. We have also performed process, voltage and temperature variation of the proposed CNFET/MTJ based 4-2 compressor. Further, in this work, we have designed a cascaded hybrid MTJ/CMOS devices and the Power, delay and power delay product have also been reported. In this work, the reliability of the proposed hybrid MTJ/CMOS 4-2 compressor is also presented.

The remainder of the paper is organized as follows: Section 2 provides a brief review of magnetic tunnel junction, 4-2 compressor and Carbon Nanotube Field Effect Transistor (CNFET). In Section 3, the proposed 4-2 compressor circuit is presented and described. The simulation and comparison results of MTJ/CMOS 4-2 compressor, MTJ/

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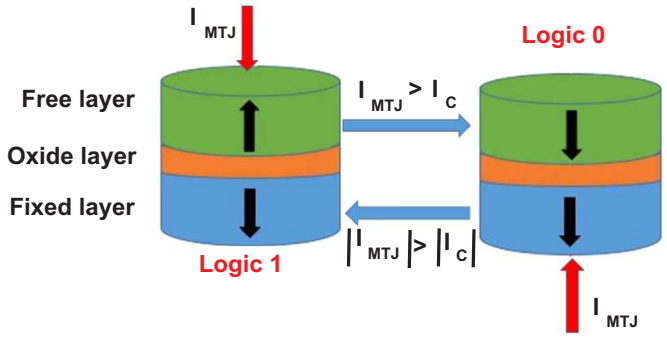

Fig. 1. Vertical Magnetic Tunnel Junction (MTJ) nanopillar structure. MTJ states change from P to AP and vice versa by applying proper current.

CNFET 4-2 compressor and the cascaded 4-2 compressor are presented in Section 4. Further, the reliability analysis of the proposed hybrid MTJ/CMOS 4-2 compressor is also presented in Section 4. Section 5 concludes the paper.

2. Background

2.1. Magnetic tunnel junction

Magnetic Tunnel Junction (MTJ) is a vertical nanopillar consists of two ferromagnetic (FM) layers and an oxide barrier [23]. In the standard application of MTJ devices, the magnetization of one of the FM layers is fixed, while the other FM layer is free to take one of the two orientations (parallel and antiparallel) as shown in Fig. 1 [19]. Depending on the orientation of the FM layers, parallel (P) or antiparallel (AP), MTJ device shows either a low resistance (RP) or high resistance (RAP) characteristic [24]. The resistance difference between the two configurations of MTJ device is given by the tunnel magnetoresistance ratio $TMR = (R_{AP} - R_P)/R_P$.

Various methods for switching MTJs have been investigated in the literature [25–29]. Among the existing methods to switch MTJs, spin transfer torque (STT) is one of the promising methods to switch MTJs [30]. Further, STT switching mechanism requires only a bidirectional current to switch the orientations in MTJs. The states of the MTJ are switched when the current of the MTJ (I_{MTJ}) becomes higher than a critical current (I_C) (Fig. 1) [31].

The MTJ based circuits are generally composed of three parts as shown in Fig. 2. The first part is the writing circuit, which is used for programing memory elements. The second part consists of STT-MRAM cells and a CMOS logic tree. STT-MRAM cells are used to store data and the CMOS logic tree is used as a logic control block. Finally, the last part is a sense amplifier (SA) that evaluates the output logic results. The pre-charged sense amplifier (PCSA) is a clock based circuit and is utilized in

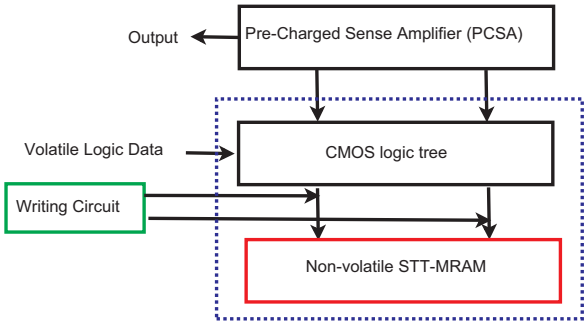

Fig. 2. Structure of a MTJ based circuit.

the MTJ based circuits because of its low power consumption and high reliability. The proposed work uses PCSA as a sense amplifier. PCSA circuit comprises of two inverters (MP1, MN1, MP2 and MN2) and two PMOS transistors MP3 and MP4 which are connected in parallel to MP1 and MP2 (Refer Fig. 4). The PCSA works in two phases depending on CLK: (i) When CLK is set to "0", the outputs (Cout, $\overline{Cout}$) are precharged to "1" (ii) when CLK is set to "1", the output voltages start discharging to ground. However, due to the difference in resistances of the different configuration of the MTJ (parallel and anti-parallel), the discharge speed will be different for each branch. For example, if the MTJ1 is configured in parallel configuration and MTJ2 is configured in anti-parallel configuration, then $R_{MTJ2} > R_{MTJ1}$. Due to the difference in resistances between R_{MTJ2} and R_{MTJ1}, the discharge current through MTJ1 will be greater than MTJ2. In the quick sequence of the discharge process, $\overline{Cout}$ will be discharged faster than Cout. When $\overline{Cout}$ becomes less than the threshold switching voltage of the inverter composed by MP2 and MN2, Cout will be charged to "1" and $\overline{C_{out}}$ will be discharged to "0".

2.2. 4-2 compressor

A 4-2 compressor is a module which has five inputs (X1, X2, X3, X4 and Cin) and three outputs (Sum, Carry and Cout). The weights of the four inputs X1, X2, X3 and X4 and the sum output are same. The weight of the carry output is one binary bit higher than the four inputs and sum. The input to the 4-2 compressor is supplied from the Cin of the preceding module of one binary bit lower. The Cout of the compressor is supplied to the next compressor module of higher significance. The fundamental equation of the 4-2 compressor is given as [32]:

$$X1 + X2 + X3 + X4 + Cin = Sum + 2(Carry + Cout) \quad (1)$$

The conventional 4-2 compressor consists of two full adder cells as shown in Fig. 3. In order to accelerate the carry-save summation of the partial products, it is important that carry output (Cout) is independent of carry input (Cin). The output functions of a 4-2 compressor are shown in Eqs. (2)–(5).

$$Cout = X1.\,X2.\,\overline{X3} + X1.\,\overline{X2}.\,X3 + \overline{X1}.\,X2.\,X3 + X1.\,X2.\,X3 \quad (2)$$

$$S = X1 \oplus X2 \oplus X3 \quad (3)$$

$$Sum = S \oplus X4 \oplus Cin = X1 \oplus X2 \oplus X3 \oplus X4 \oplus Cin \quad (4)$$

$$Carry = (Cin \oplus X4).\,S + Cin.\,X4 \quad (5)$$

2.3. Carbon Nanotube Field Effect Transistor (CNFET)

Due to the limitations of CMOS transistors, they are not able to

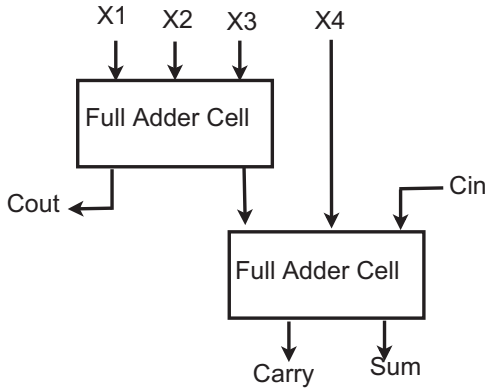

Fig. 3. Conventional 4-2 compressor structure.