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Low Power Dynamic Circuit for Power Efficient Bit lines

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Abstract: In this paper, a low power dynamic circuit is presented to reduce the power consumption of bit lines in multi-port memories. Using the proposed circuit, the voltage swing of the pull-down network is lowered to reduce the power consumption of wide fan-in gates employed in memory's bit lines. Wide fan-in OR gates are designed and simulated using the proposed dynamic circuit in 90nm CMOS technology. Simulation results show at least 40% reduction of power consumption and 1.2X noise immunity improvement compared to the conventional dynamic circuits at the same delay. Exploiting the proposed dynamic circuit, wide fan-in multiplexers are also designed. The multiplexers are simulated using a 90nm CMOS model in all process corners. The results show 41% power reduction and 27% speed improvement for the proposed 128-input multiplexer in comparison with the conventional multiplexer at the same noise immunity.

Keywords: Dynamic logic; wide fan-in gates; noise immunity; bit lines.

1. Introduction

Dynamic circuits are typically employed in read-out paths of register files and multi-port memories due to their advantages over the static ones. Main building blocks of read paths include local and global bit lines. Bit lines consume significant portion of the total dynamic power in the read-out path. As stated in [1], bit lines consume nearly 70% of the dynamic power in the register files. The power consumption of bit lines becomes the dominant factor in energy breakdown of memories as their size and number of read port are increased. Since bit lines are implemented using wide fan-in dynamic gates, power consumption of read-out paths can be reduced by using low power dynamic circuits.

A conventional dynamic circuit is shown in Fig. 1. It needs a keeper transistor to maintain the level of the dynamic node against charge sharing, leakage current and noise sources. However, delay and power consumption of the dynamic circuit increases due to the contention between the keeper transistor and the pull-down network. As the technology scaled down, the leakage current exponentially increases because of low threshold voltage and accounts for a dramatic portion of the overall power consumption [2]. This becomes even up to 50% in the 90nm technology [3]. Increasing the leakage current and crosstalk noise degrades the noise immunity, especially for wide fan-in gates due to the large number of leaky NMOS transistors connected to the dynamic node [4].

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