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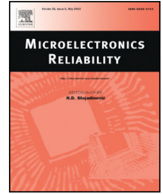

Single Event Upset rate determination for 65 nm SRAM bit-cell in LEO radiation environments

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ABSTRACT

The degradation of SRAM bit-cells designed in a 65 nm bulk CMOS technology in a Sun-Synchronous Low Earth Orbit (LEO) ionizing radiation environment is analyzed. We propose an inflight SEU rate estimation approach based on a modeled heavy ion cross section as opposed to the standard experimental characterization. Effects of irradiation with estimated LET spectrum in SRAM bit cell, i.e. the location of sensitive regions, its tendency to cause upset, magnitude and duration of transient current as well as voltage pulses were determined. It was found with SEU map that 65 nm SRAM bit-cell can flip even if high LET particle strikes in close proximity of bit-cell outside the SRAM bit-cell area. The SEU sensitive parameters required to predict SEU rate of on-board target device, i.e., 65 nm SRAM were calculated with typical aluminum spot shielding using fully physical mechanism simulation. In order to characterize the robustness of scaled CMOS devices, state of the art simulation tools such as Visual TCAD/Genius, GSEAT/Visual Particle, runSEU, were utilized whereas LEO radiation environment assessment, upset rate prediction was accomplished with the help of OMERE-TRAD software.

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1. Introduction

Non-destructive effects due to space radiation environment in on-board VLSI micro-electronic devices fabricated in very deep-sub micron (VDSM) technology nodes, also known as single event effects (SEE), are a major concern in space environments [1] Hence, the need for accurate techniques to predict radiation response of integrated circuit (IC) to ensure the reliability of its operation in space is desperately required.

The strike of energetic protons and/or heavy ions with atomic number (Z) greater than one, i.e. $Z > 1$, creates a trail of electron-hole pairs (ehps) due to ionization of silicon in semiconductor devices. These ehps propagate soon after their creation toward opposite polarity nodes due to drift and diffusion mechanism caused by electric field and concentration gradient, respectively. If the collected charge at the sensitive node is greater than its critical charge Q_{crit}, an inversion of stored value occurs in memory devices. This effect is called bit-flip or Single Event Upsets (SEU) [2,3].

In this paper, SEUs caused by heavy-ions existing at Low Earth Orbit (LEO) altitude were investigated for six-transistor (6T) Static Random Access Memory (SRAM) circuit designed in 65 nm bulk CMOS technology. The simulation of irradiation experiment was realized in Visual Particle/GSEAT module of Visual TCAD with frequently used beams of heavy ions accelerators to determine the trajectories generated by incident particles in materials for SRAM bitcell based on Monte Carlo code. Geant4 based Single Event Analysis Tool (GSEAT) is a Monte Carlo simulation tool whereas visual particle is termed as Graphic User Interface (GUI) for GSEAT. With the help of GSEAT detailed trajectories of incident particle, delta particles and the energy deposited along the trajectories were determined. Cogenda has developed semiconductor device simulator named Genius which was utilized to determine SEU related parameters and Gds2Mesh, the 3D device model builder to interface irradiated model with GSEAT. Then, runSEU program was utilized to determine the SEU cross-section for SRAM bitcell in LEO radiation environment by utilizing 3D device model and incident ion trajectories. Hence, the motivation to utilize Visual TCAD suite was the substantial foundation for SEE analysis that can be built with these above mentioned tools developed by Cogenda [4] and presented method helps to predict/

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analyze the radiation response of nano-CMOS device test vehicle based on target technology node in radiation environment.

The rest of the paper is organized as follows. Section 2 introduces the architecture of 6T SRAM designed in target 65 nm technology node. Section 3 relates with estimation of protons and heavy ions radiation environment present at LEO for two years mission period from 1st Jan 2016 to 31st Dec 2017 using the OMERE-TRAD toolkit. Section 4 presents the determination of SEU rate for 6T SRAM storage cell. Finally, Section 5 concludes this work.

2. Architecture of 6T SRAM bit-cell in 65 nm CMOS technology

Our investigation of SEU effects was performed on a 6T SRAM bit-cell in a 65 nm CMOS technology. The limitation to design a foundry specific model of device under study i.e. (6T SRAM) was unavailability of relevant process development kits (PDKs) which is proprietary to fabrication process for specific foundry. Therefore, the process technology parameters such as channel length, power supply voltage (V_{DD}), and gate dielectric material thickness were determined to establish the layout for academic model of SRAM bitcell in agreement with International Technology Road-map for Semiconductors (ITRS) for MOS circuits design for 65 nm bulk CMOS technology [5–7]. The most relevant parameters of 65 nm SRAM bitcell layout design incorporated in GDS2MESH module to generate 3D model of device are listed in Table 1.

The 6T SRAM cell consists of two cross-coupled inverters called storage bit-cell or storage latch and two NMOS access transistors known as pass-gates or access-transistors. Fig. 1 depicts the SRAM schematic.

The memory storage cell is composed of two cross-coupled inverters. Fig. 1 shows the two cross-coupled CMOS inverters (M1–M4) with two NMOS access transistors (M5, M6). It can be noted that NMOS pull-down transistors (M1, M3) and access transistor (M5, M6) share the common drains. The source regions of access transistors are connected to complementary bit-lines represented by bit-line (BL), bit-line bar (BLB) and gate terminals of access transistors are connected to word-line (WL) to turn latch in ON or OFF mode depending upon the mode of operation of SRAM. Moreover, the source regions of storage cell's NMOS as well as PMOS transistors are connected to nearest neighboring cells in SRAM array.

The arrow in Fig. 1 represents exemplary a heavy ion strike at the drain of a NMOS transistor (M3) while it is in off-state. In this case, the ion strike causes a transient change in the output voltage of (Right Hand Side) RHS inverter which appears on the input of (Left Hand Side) LHS inverter. If the voltage at the input of LHS inverter falls below the switching threshold, then the output of RHS inverter results in change of state of memory cell from high logic state "1" to low logic state "0" at node "Q". Therefore, the charge on the gate capacitance determines the state of the inverter and, consequently, the change in magnitude of the transient voltage depends on the amount of charge collected at the input node of CMOS inverter in storage cell. Typically, the vulnerability of CMOS devices to SEU is defined in terms of a critical charge, i.e., the required amount of collected charge to produce a transient voltage which is sufficient to switch the state of inverter. Therefore, it is inferred that critical charge depends on the supply voltage and on the gate/substrate capacitance of the inverter [8].

Fig. 2 shows the 3D layout of the 6T SRAM bit-cell in conformance with design rules for 65 nm process technology node. The poly-silicon gate material, two CMOS inverters with NMOS, PMOS transistors have been properly labeled.

Table 1
Design parameters for SRAM layout in bulk CMOS technology.

Parameters	Thickness	Remarks
Substrate (T_{Sub})	70 μm	Substrate thickness
Gate oxide (T_{ox})	2.45 nm	Oxide thickness
Isolation (T_{STI})	0.35 μm	Shallow trench isolation thickness
Silicide ($T_{Silicide}$)	0.02 μm	Thickness of silicide layer
Metal layer (T_{M1})	0.18 μm	Thickness of metal 1 layer
Poly-silicon gate (T_{Poly})	0.1 nm	Thickness of poly-silicon gate

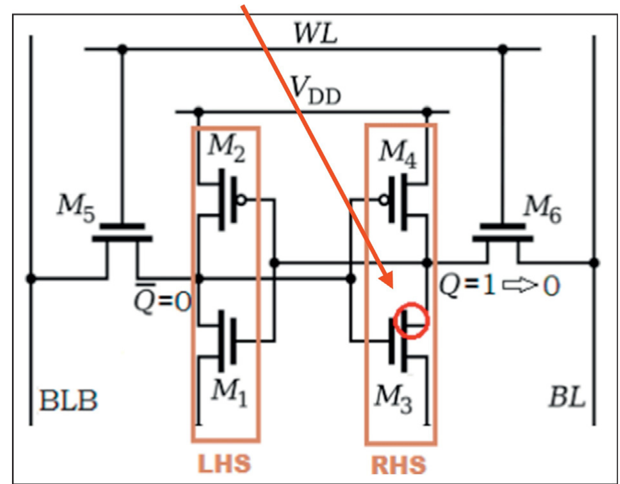

Fig. 1. Single port 6T SRAM bit-cell schematic whereas the arrow illustrates the location of a heavy ion strike.

3. Determination of radiation environment at LEO altitude

In order to assess the radiation environment existing at LEO altitude, all three main sources of ionizing radiation were considered in our analysis, i.e., the trapped electrons and protons in Van Allen earth radiation belts (ERBs), solar energetic particles (SEP) and galactic cosmic rays (GCRs) [9]. GCRs consist mainly of hadrons with fractions of protons (87%), alpha particles (12%), and heavier ions (1%) but heavy ions with Z > 26 (iron) are rare [10]. The fluxes of particles along with corresponding energy spectra can be calculated using OMERE-TRAD [11].

The energy spectra of different particle species from different sources are conveniently generalized into LET spectra, where LET is the linear energy E transfer defined as the mass stopping power of an impacting species in a media with mass density ρ [10]:

$$\mathrm{LET} = (\mathrm{d}E/\mathrm{d}x)/\rho. \tag{1}$$

The integral flux vs LET curves, shown in Fig. 3, determines the range of LET and flux of particles in sun-synchronous LEO environment, transmitted through Al shields with 100 mils thickness, to be encountered by a SRAM cell of on-board sun-synchronous satellite [12].

The fluence distribution of energetic particles drops off rapidly with increasing LETs, the largest population of particles has an LET of 20 MeV-

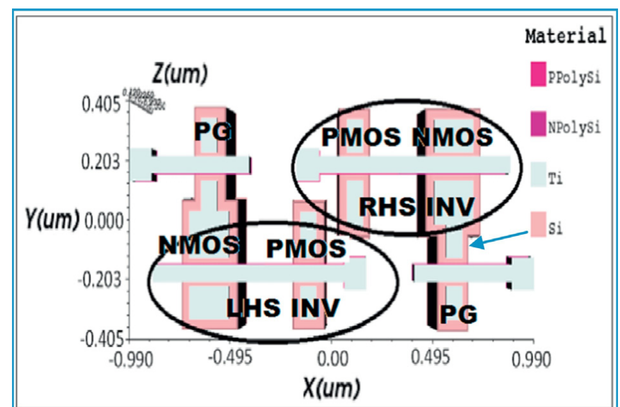

Fig. 2. 3D mask layout of 6T SRAM bit-cell in 65 nm process technology node whereas the arrow illustrates the location of a heavy ion strike.

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