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Sense amplifier comparator with offset correction for decision feedback equalization based receivers

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ABSTRACT

A decision feedback circuit with integrated offset compensation is presented in this paper. The circuit is built around the sense amplifier comparator. The loop latency is reduced by closing the feedback loop around the first stage. The feedback loop is implemented using a switched capacitor network that picks from one of pre-computed voltages to be fed back. The comparator's offset that is to be compensated for, is added in the same path. Hence, an extra offset correction input is not required. The circuit is used as a receiver for a 10 mm low swing interconnect implemented in UMC 130 nm CMOS technology. The circuit is tested at a frequency of 1 GHz and it consumes 145 μA from a 1.2 V supply at this frequency.

1. Introduction

Decision-Feedback-equalization (DFE) is a technique that compensates for intersymbol interference (ISI) in a serial input digital data signal [1–4]. Fig. 1 shows the block diagram of a DFE circuit. In this technique, a hard decision is made on the input in every clock cycle. This decision is scaled and subtracted from the input before the next sampling event. The scaling factor is chosen based on the amount of previous bit ISI in the input data. If the initial decision is correct, this effectively erases the memory of the previous bit. The delay involved in making the hard decision, scaling it and subtracting from the next input limits the maximum frequency of operation of this circuit. Further, in scaled technologies the decision devices have inherent offset that needs to be compensated for. In this paper, we propose a DFE circuit built around the Sense amplifier comparator that has low loop latency and features integrated offset compensation.

DFE is a simple technique and has found wide applications from low power to high performance communication systems. DFE has been proposed as an effective way of extending the bandwidth of repeaterless low swing interconnects [1,2]. DFE has also been used to correct for errors in digital systems [5], for implementing low power logic circuits based on pass transistor logic [6] and for enhancing bandwidth of flip-flops [7]. A sense amplifier comparator [8] is used in most of these circuits as it can achieve high speed at low power consumption. When used for sampling low swing data, these comparators need offset compensation. One of the ways of performing offset compensation is by loading the drains of the input pair with digitally programmed binary weighted capacitors [9]. However, this reduces the speed of the comparator due to the capacitive loading at this critical node. Performing offset correction with gate control of a shunt current source is a better technique as it has low parasitic capacitance [10]. This technique, of using an auxiliary input to the comparator has been used for offset correction in Refs. [2,3,11]. In high speed designs where the loop delay becomes the bottleneck, look-ahead-dfe is used [2,4]. In look-ahead-dfe, multiple comparators make decisions on the input data, each assuming a possible value of the previous decision. This increases the number of comparators needed, each requiring its own offset compensation circuit as well.

In this paper, we propose a DFE circuit that has low latency and integrated offset compensation. The feedback loop is built with a switched capacitor circuit, driven by the first stage of the sense amplifier, which picks from pre-computed inputs for the feedback. The offset to be corrected is added to the same feedback input, removing the need for an extra offset correction input to the comparator. The circuit is designed and fabricated in UMC 130 nm CMOS technology for a data rate of 1 GHz. A double differential architecture, with a differential main input and differential feedback input, is used. For testing the equalizer, the comparator is used as a receiver of a 10 mm on-chip interconnect with a capacitively coupled low swing transmitter reported by Mensink et al. in Ref. [1].

The paper is organized as follows. The concept of switched capacitor DFE with offset compensation is discussed in Section 2. The circuit implementation details are then discussed in Section 3, which is followed by results in Section 4. Section 5 then concludes the paper.

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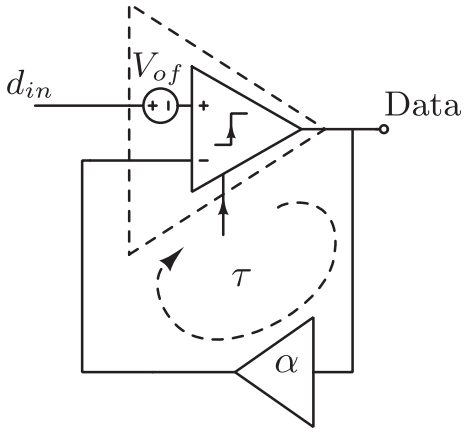

Fig. 1. Block diagram of a DFE circuit, indicating the sampler offset and the feedback loop.

2. DFE with switched capacitor feedback

In time domain, the output $y[n]$ of the DFE circuit can be expressed in terms of the comparator input $x[n]$ as

$$y[n] = Q\{x[n]\} = Q\{d_{in}[n] - \alpha y[n-1]\}$$

$$= \begin{cases} -1, & \text{if } x[n] < 0. \\ +1, & \text{otherwise.} \end{cases} \quad (1)$$

Here, $y[n-1]$ is the hard decision made by the comparator in the previous cycle and α is a constant that is less than 1. α is chosen depending on the amount of ISI present in the input data. The difference equation

$$x[n] = d_{in}[n] - \alpha y[n-1],$$

is a high pass function, which compensates for the ISI produced by the low pass nature of the interconnect. Since $y[n]$ is a hard decision, the term $\alpha y[n-1]$ can take only one of two values, i.e.

$$\alpha y[n-1] = \begin{cases} -\alpha, & \text{if } y[n-1] = -1. \\ +\alpha, & \text{if } y[n-1] = +1. \end{cases}$$

The analysis till now assumes an ideal comparator. Practically, comparators also suffer from offset, which needs to be corrected. To compensate for the inherent offset of the comparator, the offset correction V_{offset} can added within the same feedback i.e.

$$\alpha y[n-1] - V_{offset} = \begin{cases} -\alpha - V_{offset}, & \text{if } y[n-1] = -1. \\ +\alpha - V_{offset}, & \text{if } y[n-1] = +1. \end{cases}$$

We implement the DFE circuit using a switched capacitor circuit that uses the comparator output to select from pre-computed voltages that correspond to $-\alpha - V_{offset}$ and $+\alpha - V_{offset}$ for the feedback. Since most of the applications use differential input architecture, a comparator with a double differential input, i.e. with a differential main input and differential feedback input is used. Such an implementation needs two precomputed differential bias inputs with different common modes, for the feedback network to pick from. Hence, a total of 4 distinct bias voltages are needed. This is explained in the following.

When $y[n-1] = +1$, the differential feedback voltages V_{fb}^{+}, V_{fb}^{-} can be written as

$$V_{fb}^{+} = V_H^1 = V_{cm} + \frac{V_{offset}}{2} + \frac{\alpha}{2},$$

$$V_{fb}^{-} = V_L^2 = V_{cm} - \frac{V_{offset}}{2} - \frac{\alpha}{2}.$$

Similarly, $y[n-1] = -1$,

$$V_{fb}^{+} = V_L^1 = V_{cm} + \frac{V_{offset}}{2} - \frac{\alpha}{2},$$

$$V_{fb}^{-} = V_H^2 = V_{cm} - \frac{V_{offset}}{2} + \frac{\alpha}{2}.$$

Here, V_{cm} is the common mode of the feedback input. This is illustrated graphically in Fig. 2, along with the block diagram of the comparator with a double differential input.

To summarize, the voltages V_H^1, V_L^1, V_H^2 and V_L^2 are the four feedback bias voltages. The difference $V_H^1 - V_L^1$ $(= V_H^2 - V_L^2)$ corresponds to the feedback factor α. The common modes of these two differential pairs are skewed by the offset to be corrected, as illustrated in Fig. 2.

We use the sense amplifier based comparator in the DFE circuit. The circuit diagram of the first stage of the comparator is shown in Fig. 3. An additional input transistor pair is used for the feedback input [3].

The second stage of the comparator is an SR slave latch [8]. Prior implementations of DFE using this comparator have used the slave latch output for the decision feedback [1]. We use the first stage output itself for the feedback, which results in minimum latency. The nodes $\overline{S}$ and $\overline{R}$ are precharged in every cycle to V_{DD}. During the input evaluation phase, these nodes discharge through the input transistors and depending on the input, one of the nodes discharges faster than the other. When $\overline{S}$ and $\overline{R}$ are discharged below the trip point of the inverters formed by M_p^1, M_n^1 and M_p^2, M_n^2, the inverter positive feedback pulls $\overline{S}$ and $\overline{R}$ apart in the direction established by the input pair. Typical waveforms of $\overline{S}$ and $\overline{R}$ are shown in Fig. 4. The output of the first stage is used to drive a switched capacitor network which picks from the two pairs of differential bias voltages for the feedback. This effectively results in a low swing dynamic latch for the decision feedback. The circuit implementation is discussed in the next section.

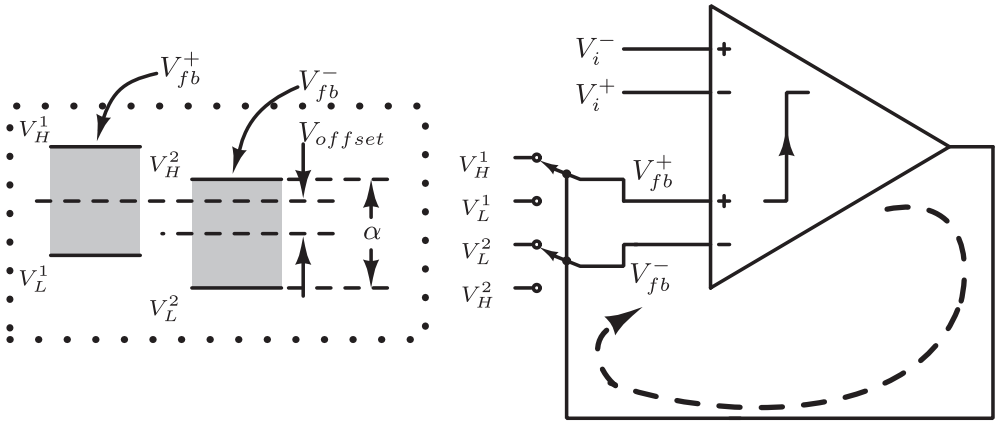

Fig. 2. Conceptual block diagram of the DFE circuit with offset correction. The circuit has a differential main input and a differential feedback input.