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## Bubbling in a power electronic inverter: Onset, development and detection



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#### a r t i c l e i n f o

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#### a b s t r a c t

Power electronic DC/AC converters (inverters) play an important role in modern power engineering for a broad variety of applications including solar and wind energy systems as well as electric and hybrid cars drives. It is well known that the waveform of the output voltage (or current) of an inverter may be significantly distorted by phase restricted high frequency oscillations, frequently referred to as bubbling. However, the reasons leading to the appearance of this undesired effect are still not completely understood. Considering as an example a 2D model of a PWM H-bridge single-phase inverter, the present paper reports the appearance of two different kinds of bubbling. In the first case, the appearance of bubbling occurs suddenly and is related to the change of periodicity. We show that high-periodic, quasiperiodic and chaotic oscillations may exhibit bubbling, and also that solutions with and without bubbling may coexist. In the second case, the appearance of bubbling occurs gradually in the parameter domain where the investigated system undergoes border collisions of so-called persistence type. As a result, the appearance of the bubbling of the second kind does not change the periodicity of the motion but nevertheless disturbs the waveform. We discuss some differences in the properties of the second kind of bubbling from the first one, and present numerical techniques for its detection.

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#### **1. Introduction**

The purpose of a DC/AC converter is to provide an AC output waveform from a DC power supply  $[1]$ . Converters of this type (also known as inverters) are widely used both in the industry and in private households. Examples of their applications include uninterruptable power supplies (UPS), active filters, flexible AC transmission systems (FACTS), voltage compensators, adjustable speed drives (ASDs), backup systems for sensitive computers and hospital equipment [\[1\].](#page--1-0) Moreover, in the last years a worldwide growing interest in renewable energy sources (solar photovoltaic and wind energy systems)  $[2-6]$  as well as in electric and hybrid car drives [\[7\]](#page--1-0) led to an increasing interest in DC/AC converters. Indeed, inverters are inherent parts of all these systems, so that understanding their dynamic behavior is highly demanded in order to identify

parameter settings leading to a desired robust behavior according to specific industrial requirements and to predict possible undesired effects.

Operation of an inverter system is characterized by a cyclic switching of the circuit topology. The switching process is controlled through a feedback mechanism by the sinusoidal pulsewidth modulation (PWM). Like models of other systems with switching control, mathematical models of DC/AC converters belong to the class of piecewise-smooth systems. In this way the dynamics of an inverter is governed by two strongly different frequencies, namely by the low frequency of a reference sinusoidal signal (which determines the frequency and the phase of the desired output signal) and a high switching frequency. Therefore, as shown in  $[8-10]$ , modeling of DC/AC converters leads to a class of piecewise-smooth systems not completely covered by the existing theory. A distinguishing feature of these models (stroboscopic maps) is an extremely high and practically unpredictable number of switching manifolds (borders in the state space). This leads to a variety of unusual bifurcation structures, such as transitions to chaos via irregular cascades of border collisions [\[8\]](#page--1-0) as well as

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structures formed by so-called persistence border collisions inside the stability domain of a fixed point  $[9]$ , and a global alignment of smooth bifurcation boundaries [\[10\].](#page--1-0)

The desired mode of operation of an inverter is given by stable sinusoidal oscillations (corresponding to a stable and preferably a globally attracting fixed point of a suitable stroboscopic map) with the frequency prescribed by an external reference signal. Clearly, such an ideal signal is always overloaded by high frequency low amplitude oscillations caused by the switching process. However, under certain conditions, the output signal is additionally distorted by some undesired effects. Among such effects, the *bubbling* phenomenon, i.e. suddenly appearing phase-dependent high frequency small amplitude oscillations modulated by a low frequency power mode, is one of the challenging unsolved problems in the dynamics of inverters (as well as in AC/DC converters whose dynamics is also determined by two frequencies). Note that in the literature, the term "bubbling" is used for different phenomena. Here we use it in the following sense: for a signal showing low frequency oscillations the bubbling phenomenon means that the signal is distorted by high frequency oscillations existing in a short phase interval and not existing (or at least not visible) elsewhere [\[11,12\].](#page--1-0) Different meanings of the term used in  $[13-16]$  are not relevant for our work. Note also that following  $[12,17-19]$  the bifurcation leading to bubbling phenomenon is frequently called a "fast scale bifurcation" or even a "fast scale period-doubling bifurcation" [\[20\],](#page--1-0) or "period-bubbling" [\[21\].](#page--1-0) This is certainly not correct in general, as the period of the overall signal after this bifurcation may not only be doubled but also may be kept unchanged (see an example in  $[9]$ ); the signal may also become quasiperiodic  $[22]$ .

The bubbling phenomenon has been reported for the first time for DC/DC converters  $[11,23]$ . The mechanisms leading to its appearance were investigated numerically and experimentally by many authors [\[12,17–22,24–26\].](#page--1-0) Unfortunately, the presented partial explanations contradict each other in many aspects, the obtained numerous experimental results are not systematized, and there is still no satisfactory theory explaining the appearance of the bubbling effect. Recently, many publications devoted to bubbling in AC-DC converters appeared [12,27-33]. Since these systems have a varying input voltage, their discrete-time models belong to the same class of piecewise-smooth systems with a high number of borders as the one considered in the present work (see [\[26\]](#page--1-0) for details).

The existing publications on bubbling in inverter systems are by far not so numerous. The existence of this phenomenon in a fullbridge inverter has been demonstrated both numerically and experimentally in [\[20,25\].](#page--1-0) In [\[21\]](#page--1-0) a 3D-model of an H-bridge inverter demonstrating the bubbling phenomenon and an experimental verification of this behavior are reported.

As a matter of fact, the general reasons leading to the appearance of bubbling are still unknown, which is a serious problem for applications, as high frequency oscillations lead to a significant distortion of the output waveform. The purpose of the present paper is to contribute to the investigation of the bubbling phenomenon in inverter systems. Note that at the present stage we do not aim to provide any general conditions leading to the appearance of bubbling. Instead, as a preliminary step, we ask the questions which kinds of bubbling are possible and how bubbling of different kinds appear.

The paper is organized as follows. In Section 2 we introduce the considered model, first in the continuous and eventually in the discrete time. In [Section](#page--1-0) 3 the bifurcation structure in the considered parameter plane is presented and the regions of interest in this plane are identified. The following [Section](#page--1-0) 4 is devoted to the main object of this paper, i.e., to the bubbling phenomenon. In [Section](#page--1-0) 4.1 we discuss the appearance of bubbling associated with a changing periodicity (in particular, with the appearance of quasiperiodicity) and possibly with multistability. In [Section](#page--1-0) 4.2 a different kind of bubbling is reported, which does not change the periodicity of the signals but leads to the distortion of their waveform. Clearly, a numerical detection of bubbling in this case is a more sophisticated task than in the case of changing periodicity. Two possible solutions to this task are suggested in [Section](#page--1-0) 4.3. Thereafter, in [Section](#page--1-0) 4.4 the question is discussed how the bubbling effect influences the structure in the parameter space formed by persistence border collision boundaries. Finally, the presented results are summarized in [Section](#page--1-0) 5.

#### **2. Description of the system**

[Fig.](#page--1-0) 1(a) shows a schematic diagram of the considered pulse-width modulated H-bridge single phase inverter and [Fig.](#page--1-0) 1(b) illustrates the generation of the signal used to control the four switches  $S_1 - S_4$ .

In [Fig.](#page--1-0) 1(a), *L* and *C* denote, respectively, the inductance and the capacitance of the *LC* filter,  $R_L$  is the load resistance, and *R* is a parasitic resistance characterizing the dissipation in the system associated, for instance, with the equivalent resistance of the open transistor switches, the internal resistance of the DC power source, and the series resistance of the inductance coil. The variable  $x_1$  represents the current in the filter inductance  $L$  and  $x_2$  is the output voltage.

The four switches of the bridge structure operate in pairs such that  $S_1$  and  $S_4$  are closed when  $S_2$  and  $S_3$  are open, and *vice versa*. When  $S_1$ ,  $S_4$  are on and  $S_2$ ,  $S_3$  are off, a positive voltage  $E_0$  is applied to the load, and when  $S_1$ ,  $S_4$  are off and  $S_2$ ,  $S_3$  are on, this voltage is reversed. The switches are controlled by the sinusoidal PWM modulator through a feedback mechanism. In order to generate the control signals to the switches  $S_1$ ,  $S_4$  and  $S_2$ , *S*3, the corrector amplifier *DA*<sup>2</sup> determines first the error signal  $\xi(t) = \alpha(V_{\text{ref}}(t) - V_{\text{s}}(t))$  that measures the difference between the reference sinusoidal voltage  $V_{ref}(t) = V_m \cdot \cos(2\pi t/T)$  and the output signal  $V_s(t) = \beta x_2(t)$  of the voltage sensor *VS*. Here,  $\alpha$  is the corrector gain factor and  $\beta$  is the voltage sensor sensitivity;  $V_m$  and  $T = ma$  are the amplitude and the period of the reference signal, respectively. The parameter *a* denotes the ramp period (the period of the clock signal  $V_{clock}$ ) and *m* is referred to as the frequency modulation ratio, i.e., the number of clock cycles during the period *T* of the reference signal. In the following, *m* is assumed to be an integer number. The frequency modulation ratio *m* plays an important role in determining the accuracy with which the reference signal can be reproduced by the load voltage.

As illustrated in [Fig.](#page--1-0) 1(b), the sample-and-hold unit *S*/*H* reads the error signal  $\xi(t)$  at every clock time  $t = ka$ ,  $k = 0, 1, 2, \ldots$ , and maintains it for the following switching period. This produces the control signal  $V_{\text{con}}(t)$ . Finally the comparator  $DA_1$  compares this control signal from the sample-and-hold unit with the periodic ramp function  $V_{ramp}(t)$  and generates the control signals to the switches  $S_1$ ,  $S_4$ , and  $S_2$ ,  $S_3$ . As long as  $V_{\text{con}}(t) > V_{\text{ramp}}(t)$ , switches *S*<sub>1</sub>, *S*<sub>4</sub> are on and *S*<sub>2</sub>, *S*<sub>3</sub> are off, while for  $V_{con}(t) \leq V_{ramp}(t) S_1$ , *S*<sub>4</sub> are off and  $S_2$ ,  $S_3$  on. This type of modulation is also known as pulse-width modulation of the first kind.

The ramp function  $V_{\text{ramp}}(t)$  varies from  $-V_0$  to  $+V_0$  in synchrony with the clock signal  $V_{clock}$ . If  $V_{con}(t) \geq +V_0$  or  $V_{con}(t) \leq -V_0$  the modulator is saturated. In the first case, i.e., if  $V_{con}(t) \geq +V_0$ , the duration of the positive pulse is equal to the ramp period *a*, and in the second case, i.e.,  $V_{con}(t) \leq -V_0$  it is equal to zero.

#### *2.1. Model in continuous time*

The dynamics of the PWM H-bridge inverter described above can be represented by the following 2D non-autonomous

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