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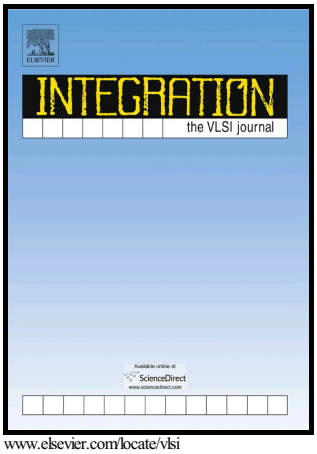


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# Boundary Optimization of Buffered Clock Trees for Low Power

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***Abstract*—The work solves a new problem of optimizing the boundary of buffered clock trees, which has not been addressed in the design automation as yet. Precisely, we want to show that the clock cells that directly drive flip-flops should not necessarily be buffers. By taking into account the internal structure of flip-flops, we can have a freedom of choosing either buffers or inverters for the cell implementation from library. This in fact leads to cancel out the two inverters, one in the driving buffer and another in each flip-flop, thereby reducing the power consumption on the clock tree, including flip-flops. We generalize this idea to look into the possibility of co-optimizing the driving buffers and flip-flops together to reduce the clock power at the boundary of clock trees, and propose an effective four-step synthesis algorithm of clock tree boundary for low power. By applying our proposed technique to benchmark circuits, it is observed that the clock power is able to be reduced by 4.45%∼6.33% further on average without timing violation.**

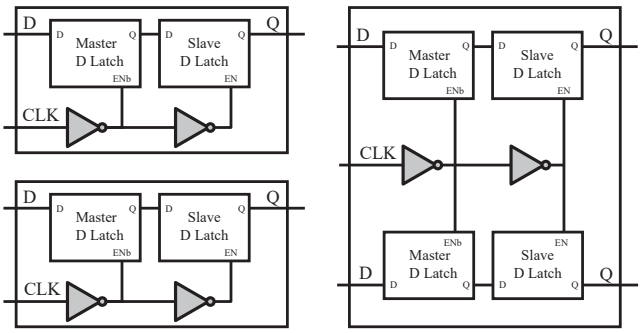
**Keywords**: Clock tree synthesis, buffered clock tree, low power, post-placement optimization.

## I. Introduction

Reducing power consumption has become a major concern in designing most of the modern VLSI systems. Among a lot of sources, clock takes significant amount of portion of the dynamic power consumption. The power consumption mainly comes from the switching of clock signals by the inverters that compose the clock buffers. This work focuses on restructuring the clock buffers combined with the inverters in the flip-flops, so that the total number of inverters inside the buffers and flip-flops is reduced, thereby reducing clock power with no timing violation.

Various techniques of effectively optimizing a clock tree for reducing clock power have been proposed. The source of power consumed on clock trees consists of two parts: (1) power consumed by wire capacitance and (2) power consumed by switching on flip-flops. Because of these two factors, lots of research efforts have been made on the optimization of clock wires, clock buffers, and flip-flops. A buffer plays an important role on a clock tree not only in controlling timing (i.e., clock skew) but also controlling clock power. By inserting a buffer to a long clock wire in a clock tree, a clock wire can have smaller capacitance because of its shortened wire segment that is driven by the inserted buffer, which leads to amplify clock signal and reduce the clock power.

Pullela, Menezes, and Pillage [1] showed that inserting buffers to clock trees, in spite of the additional power dissipation due to their short-circuit currents, can significantly reduce the clock tree power, given the constraint on allowable process-variation-dependent clock skew. Xi and Dai [2] proposed a buffer insertion and sizing method to induce very small skew in the loads and wire width variations of the resulting small clock subtrees to enable the use of minimal wire widths, so that minimal wiring capacitance and power consumption can be achieved under clock skew constraint. They also tried to reduce the clock power further by adjusting the NMOS and PMOS transistors in buffers under process variation. Lillis, Cheng, and Lin [3] proposed a (power-minimal) optimal algorithm of discrete wire sizing and buffer insertion. One unrealistic assumption of the work is that they assumed the intrinsic delay of every buffer of various size is identical. In [4], Vittal and Marek-Sadowska proposed an algorithm of generating clock tree topology and inserting buffers simultaneously. They formulated the problem as minimizing the total power dissipated by buffers and wires under clock skew and rise time constraints, in which the *deferred merge embedding* [5] technique was embedded with buffer insertion in their flow. By modeling into the equivalent circuit, they find some regions where a buffer can be placed to meet zero-skew condition. Recently, Pan, Chu, and Chang [6] introduced a dynamic programming based H-clock tree construction algorithm with buffer library under the transition time bound. To make the search space not to be large, a proper pruning scheme was given. They concluded that as the transition time bound is much tighter, consumed power gets higher. Rakai *et al.* [7] introduced geometric programming for buffer sizing on a clock tree while considering process variation.




(a) 1-bit flip-flops (b) 2-bit flip-flop

Fig. 1. Internal structure of 1-bit master-slave based flip-flops and 2-bit flip-flop in which the pairs of master-slave latches share the clock driving logic.

On the other hand, there are a number of works that have addressed the synthesis and optimization of flip-flops to save clock power. Deng, Cai, and Zhou [8] proposed a