Electric Power Systems Research 148 (2017) 97–107

Contents lists available at ScienceDirect

Electric Power Systems Research

journal homepage: www.elsevier.com/locate/epsr

A voltage level based predictive direct power control for modular multilevel converter

Sze Sing Lee [a,b,*], Yeh En Heng [b]

[a] EEE Research Group, School of Electronics and Computer Science (ECS), Faculty of Physical Sciences and Engineering, University of Southampton, Southampton, United Kingdom
[b] University of Southampton Malaysia Campus, Nusajaya, Johor, Malaysia

ARTICLE INFO

Article history:
Received 22 December 2016
Received in revised form 19 February 2017
Accepted 24 March 2017

Keywords:
Modular multilevel converter (MMC)
Predictive control
Direct power control
Circulating current control
Capacitor voltage balancing

ABSTRACT

This paper proposes a novel voltage level-based predictive direct power control (PDPC) strategy integrated with voltage sorting algorithm for a three phase grid-connected modular multilevel converter (MMC). The main advantage of the proposed control strategy, compared with the predictive current controllers, is that it does not need angular information of grid parameters. Therefore, it is simpler and able to get rid of rotary transformation and inner current loop. Contrary to the phase-by-phase control in predictive current controllers, the proposed control scheme advocates three-phase control. As a result, it achieves significant improvement in terms of smaller power ripples, more accurate tracking of power references, and less current harmonics. Further study reveals that the proposed voltage level-based PDPC exhibits less switching frequency irrespective of the magnitude of power references and power angles. Meanwhile, the capability of capacitor voltage balancing control and circulating current control in the proposed PDPC is as good as in the predictive current controllers. Some in-depth simulation comparisons with one of the existing predictive current controllers are given to validate the effectiveness of the proposed strategy.

1. Introduction

The topology of modular multilevel converter (MMC) was first introduced in 2003 [1]. Since then, there has been tremendous surge in research of employing MMC in medium or high voltage applications such as battery energy storage system [2], high-voltage-direct-current (HVDC) transmission [3–5], medium-voltage distribution networks [6], static synchronous compensator (STATCOM) [7,8], and etc. The impressive and successful penetration of MMC into high voltage applications is mainly attributed to its modularity and scalability to cater for any voltage level demands [9]. To date, the control strategies for MMC are mostly limited to classical linear control and pulse width modulation (PWM) [10–13]. Nonetheless, in recent years, significant research concerning the MMC control have been diverted to the model predictive control (MPC) which features simplicity, easy inclusion of nonlinearities, ease in digital implementation, and fast dynamic response [14]. The high flexibility of MPC in concurrent manipulation of control objectives made it particularly appealing in MMC topology.

Among the different MPCs, finite control set MPC (FCS-MPC) is gaining particular attention as the optimization problem is solved from a discrete model of the system. It superseded conventional methods in the research of power converters and it is progressively matured and receive wider acceptance. It is worth mention that the implementation of FCS-MPC to MMC is fairly recent. The idea of applying FCS-MPC current control approach into grid-connected MMC was first proposed in Ref. [15] and was verified its effectiveness in power flow regulation, capacitor voltage balancing, and circulating current minimization. However, the FCS-MPC current controller retained the conventional way of rolling optimization where the cost function is evaluated by all possible switching states [16]. The switching states tends to increase as the number of level increases, which in turn gives rise to more intense computational burden. For instance, with N refers to the number of submodules (SMs) per arm, the MMC can produce either $N+1$ or $2N+1$ output voltage levels. The former imposes limit on the number of SMs inserted in the phase to N while the latter allows the number of SMs inserted in the phase varies up to $2N$. A total of C_{2N}^{N} switching states are available for $(N+1)$ level MMC for each phase [15]. For $(2N+1)$ level MMC, the accessible switching states increased dramatically to 2^{2N} [17]. Recently, switching states grouping [18] and dual-stage cascaded control strategy [19] are proposed to decrease the computational burden. Nonetheless, these approaches can only alleviate

* Corresponding author.
E-mail address: ss.lee@soton.ac.uk (S.S. Lee).

http://dx.doi.org/10.1016/j.epsr.2017.03.023
0378-7796/

the computational burden to some extent and suitable only for N with small values.

Another most commonly used approach in reducing computational burden is the voltage level-based FCS-MPC current control strategy. The main motivation of voltage level-based FCS-MPC current control is to distribute the multiple objectives into separate controllers. In other word, the total computational burden is no more sustained by a single central controller, but portioned out to one or more local controllers. For instance, the MPC central controller in Refs. [20–25] is accountable for the control of ac-side current and circulating current while a local controller which is based on voltage sorting algorithm is dedicated to the task of capacitor voltage balancing. The capacitor voltages for upper and lower arms are sorted according to the current polarity. All the possible switching-on pairs for the sorted submodules will then be evaluated in the cost function [21,22]. On the contrary, Refs. [20,23,24] proposed the execution of cost function prior to the voltage sorting algorithm. The main feature of these voltage level-based FCS-MPC current controls is that the minimization of cost function is carried out by evaluating the number of voltage levels, instead of switching states. In this instance, the number of options reduced to $N+1$ for $(N+1)$ level and $(N+1)^2$ for $(2N+1)$ level. In a rather different alternative [26], the control objectives are controlled individually by three MPC controllers. Three cost functions are defined for the control of ac-current, circulating current, and capacitor voltage balancing respectively. The proposed approach is free of tuning work since weighting factor is not essential. Several attempts have been made to further reduce the computational burden, such as considering only one level change based on previous voltage level [20,23], group-sorting [27], or imposing limitation on the number of inserted submodules [24].

Predictive direct power control (PDPC) is another emerging powerful control scheme which is found increasing trend of interest in the control of grid connected converters [28–30]. Compared to FCS-MPC current control, it is simpler since it require neither an internal current control loop nor rotary coordinate transformation. It features decoupled active and reactive power control, strong robustness, and quick dynamic response [28]. Similar to the FCS-MPC current control, the PDPC generates a finite number of control actions induced by the finite number of switching states. Therefore, it is also regarded as a FCS-MPC strategy. The fundamental difference between the FCS-MPC current control and the PDPC is that the former deals with indirect regulation of power by minimizing the current control error while the latter concerns with direct regulation of power by minimizing the active and reactive power control error. So far, no work has ever investigate the performance of PDPC for MMC.

In the light of the above considerations, this paper takes the initiative in developing PDPC for grid-connected MMC. The PDPC bears some resemblance to the FCS-MPC current control such that the expressions for circulating current and capacitor voltage are remained in *abc* reference frame, but the computation of power necessitates the grid parameter variables expressed in $\alpha\beta$ reference frame. In this instance, phase-by-phase control in FCS-MPC current control is not viable since the controls among the phases become closely related. Rather than three cost functions which consider per-phase options, the PDPC involves single cost function which considers the combination of three-phase options. Greater computational burden is expected. More precisely, the three-phase possible options in PDPC is the perfect cube of the per-phase possible options in FCS-MPC current control. For example, when considering MMC with (N+1) level, the available combination of options for a three-phase MMC are $(C_{2N}^{N})^3$ and $(N+1)^3$ respectively if switching states and voltage levels are considered.

Table 1 summarizes the number of possible options for different FCS-MPC strategies mentioned before. Noted that the switching state-based FCS-MPC strategies are not practically applicable even if the N is of small values. On the other hand, the introduction of voltage sorting algorithm into the voltage level-based FCS-MPC strategies reduced the number of possible options to a great extent. Despite the use of voltage sorting algorithm will result in relatively sluggish dynamic response and unnecessary switching states [20,27], it remains a favorable choice in FCS-MPC of MMC since it offers the advantage of much lower computational burden of central controller which provide more possibility to real-time implementation.

On that account, the proposed PDPC opts for voltage level-based PDPC for practical consideration. The voltage level-based PDPC exhibits greater computational complexity when compared to voltage level-based current control, but much lower computational complexity when compared to switching state-based current control. Performance comparison of the proposed PDPC and voltage level-based current control in Ref. [20] for a MMC with $N=10$ is studied in this work. The remainder of this paper is organized as follows. Section 2 discusses the topology and mathematical model for a three phase grid connected MMC. In Section 3, consideration is given to present the principle of the proposed PDPC where power flow can be directly controlled and sorting algorithm is adopted. The detailed description of the block diagram of the proposed PDPC is then given. Simulation studies of the system behaviors in terms of power ripples, power tracking accuracy, capacitor voltage ripples, circulating current ripples, and average switching frequency are included in Section 4. In-depth comparative numerical studies between the proposed PDPC and voltage level-based current control in Ref. [20] are carried out. Emphasis is then placed on investigation of the robustness of the proposed PDPC against the grid parameter mismatch. Finally, Section 5 draws the conclusions.

2. Mathematical model of MMC

Fig. 1 shows the circuit configuration of a three-phase MMC connected to the utility grid through a series-connected inductor and resistor. The upper arm and lower arm of each phase leg comprise of N series connected submodules (SM). Each SM consists of a dc capacitor and two IGBTs that form a half-bridge. It should be noted that both the IGBTs are operating in complementary mode which take on binary values of either '0' or '1'. Therefore, the SM has two modes of operation, i.e. bypass mode and switched-in mode. When the lower switch is turned ON, the SM is in bypass mode with output voltage equals to zero. In contrast, when the upper switch is turned ON, the SM is in switched-in mode with its output voltage equals to the capacitor voltage v_c. In switched-in mode, the capacitor is either charging or discharging, depending on the current direction. Parameters related to upper arm are denoted by subscript 'u' while that related to lower arm are denoted by subscript 'l'. The two arm inductors L_{arm} in each phase play an important role in suppressing the circulating current between the phase legs and dc link.

By applying the Kirchoff's voltage law to the circuit diagram in Fig. 1, the dynamic behavior of MMC for phase j are obtained as:

$$\frac{V_{dc}}{2} = v_{u,j} + R_{arm} i_{u,j} + L_{arm} \frac{di_{u,j}}{dt} - R_g i_j - L_g \frac{di_j}{dt} + v_{g,j} \tag{1}$$

$$-\frac{V_{dc}}{2} = -v_{l,j} - R_{arm} i_{l,j} - L_{arm} \frac{di_{l,j}}{dt} - R_g i_j - L_g \frac{di_j}{dt} + v_{g,j} \tag{2}$$

where V_{dc} is the dc side voltage, $v_{g,j}$ is the grid voltage, $v_{u,j}$ and $v_{l,j}$ denote the upper arm voltage and lower arm voltage respectively, R_{arm} and L_{arm} represent the arm resistance and inductance respectively while R_g and L_g represent the grid side resistance and inductance respectively. On the other hand, the expressions for