Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs

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\textbf{A B S T R A C T}

Silicon carbide (SiC) based metal-oxide semiconductor-field-effect-transistors (MOSFETs) are increasingly entering the high power device market. Besides all the well-known benefits which come along with these new generations of switches, the nature of the wide bandgap material and the different properties of the semiconductor-dielectric interface involve some natural peculiarities in threshold voltage variation and bias-temperature-instability (BTI) which differ from comparable silicon (Si) MOSFET counterparts and which need to be understood and assessed. The target of this paper is to highlight such differences, explain their relation to the semiconductor material, challenge their relevance for the application and define their consequences with regard to datasheet specifications. Most of the new effects can be understood by means of simple physical models and do not compromise the reliability of the device. However, it turns out that the standard test procedures typically used to characterize threshold voltage and threshold voltage drifts for Si devices need to be adapted for SiC MOSFETs. A new measure-stress-measure procedure for BTI evaluation of SiC MOSFETs is proposed which allows distinguishing between reversible threshold voltage hysteresis and more permanent threshold voltage drift (BTI). The measurement pattern is then used to assess the $V_{th}$ stability of recently launched SiC MOSFET parts. The tested devices differ considerably in BTI drift amplitude and drift variation. The differences are attributed to variations in device processing and device design.

1. Introduction

High voltage switches based on silicon carbide (SiC) are becoming mainstream. In particular for voltage classes above 600 V, SiC technologies promise considerably enhanced performance compared to silicon based metal-oxide-semiconductor-field-effect-transistors (MOSFETs)\textsuperscript{[1,2]}. SiC MOSFETs provide significantly reduced static and dynamic losses and can be operated at higher temperature, higher power density and higher frequency. These features have clear system benefits. Operation at higher frequencies with lower losses allows shrinking passive components of inverter integrated circuits (ICs) as well as heat sinks making full SiC system solutions much lighter, more compact, cheaper and more efficient\textsuperscript{[3,4]}. Despite of all these well-known benefits it took 10 years after successful market launch of SiC diodes in 2001 by Infineon\textsuperscript{[3]} until the first productive SiC MOSFETs were launched by Rohm and Cree (today Wolfspeed) in 2011/2012. Between 2012 and 2016 several other device manufacturers such as ST Microelectronics, Microsemi and others have further enriched the portfolio of SiC MOSFET technologies on the market. These first generation devices were all planar n-channel DMOS technologies based on 4H-SiC with the SiC/SiO$_2$ interface at the Si-face of the (0001) plane. Since very recently Rohm and Infineon have launched the first SiC trench-MOSFET devices\textsuperscript{[5,6]}. The trench technology allows for higher packing density and smaller pitch size. Furthermore, it was shown that the vertical crystal planes of 4H-SiC provide higher channel mobilities in comparison to the planar (0001) planes\textsuperscript{[7]}. Both advantages improve device performance and reduce the on-resistance times active area ratio ($R_{on} \times A_{act}$). Thus, despite higher fabrication complexity it is very likely that trench topologies are the future of SiC MOSFETs.

One could wonder why it took more than 15 years until SiC MOSFETs have evolved into a mature productive technology. One reason can be surely found in SiC specific manufacturing challenges. Examples are enhanced wafer roughness and wafer bow, smaller wafer diameter, transparency and hardness of the material as well as the need for developing new fabrication processes such as high temperature doping activation anneals, ohmic contact formation and new interface passivation schemes. Furthermore, before a product can be launched, it has to be proven that the technology meets industrial and/or

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Furthermore, a measurement procedure will be suggested allowing the and relevance of threshold voltage instabilities in Si and SiC MOSFETs. We will discuss di

discussed in detail in the following sections. Most of these new features and peculiarities in threshold voltage variations of SiC MOSFETs had to be developed. Naturally, di

which only exist in SiC[10,11,12]. To passivate those new defect types, different interface properties cause new features in the transfer characteristics of SiC MOSFETs which will be discussed in detail in the following sections. Most of these new features can be understood by means of simplified physical models which allow a better understanding of process dependencies and help to properly setup and assess the results of lifetime tests.

One target of this paper is to highlight and help to understand new features and peculiarities in threshold voltage variations of SiC MOSFETs. We will discuss differences and similarities in origin, effect and relevance of threshold voltage instabilities in Si and SiC MOSFETs. Furthermore, a measurement procedure will be suggested allowing the assessment of application relevant components in the total $V_{TH}$ drift in a defined and reproducible manner. In the last section of the paper the procedure is used to compare $V_{TH}$ instabilities of recent productive technologies of three different SiC MOSFET manufacturers.

2. Relevance of BTI for Si and SiC MOSFETs

In view of the operation of a MOSFET, intrinsic BTI may affect the device performance in two different ways: (i) BTI causes a parallel shift of the transfer characteristics and (ii) BTI degrades the slope of the transfer characteristic.

Independent of the technology (Si or SiC), the consequences for n-channel MOSFETs are the following

(i) Electron trapping during positive BTI stress causes a positive drift in threshold voltage thereby reducing the drain current in the on-state. On the other hand, hole trapping during negative BTI stress causes a negative drift in threshold voltage which may lead to parasitic turn-on of the device in the off-state.

(ii) If precursor sites are depassivated during BTI stress they may act as additional charge trapping and/or scattering centers. Consequently, the channel mobility can be reduced which degrades the drain current in the on-state.

For Si devices it is known that n- and p-channel MOSFETs show different BTI. This causes particular problems for complementary MOS (CMOS) circuits where both device types are used at the same time in one system. BTI and transconductance degradation ultimately affect the operating frequency and lead to a speed reduction of CMOS circuits and ring oscillators [13,14]. In sub-22 nm technology nodes SiO2 has been replaced by alternative dielectrics such as SION or high-k materials. Such insulators are known to show enhanced BTI. In these fields (and some other niche applications) BTI is still a serious reliability concern even for Si MOSFETs.

The applications of SiC MOSFETs are very different to logic IC Si devices. Typical application fields of SiC MOSFETs are motor drives, inverters, converters, switch mode power supplies, induction heating systems and photovoltaics. All these applications require high power densities and blocking voltages beyond 600 V. Today this market is dominated by Si device technologies such as CoolMOS™ and IGBT which hardly show any intrinsic BTI. However, in the near future some of these applications will be served by hybrid and/or full SiC solutions to increase performance and reduce system costs. In order to accomplish a smooth transition from Si to SiC technologies, it is important to assess the impact and relevance of BTI for such applications and understand differences between SiC and Si technologies. In the following it will be discussed how BTI induced threshold voltage drifts could possibly affect the reliability and performance of high power devices and integrated systems:

i. High power devices are often connected in parallel in modules to enhance the maximum current. The efficiency of parallelization depends on the matching of the on-resistance and threshold voltage of the individual devices. Irregular $V_{TH}$ degradation due to BTI may lead to inhomogeneous current distributions within the system. As a result, the commutation efficiency degrades and the module temperature increases.

ii. A gradual positive drift of the threshold voltage reduces the overdrive in the on-state. As a consequence, the channel resistance of single devices is increased which degrades the efficiency and enhances static losses and the module temperature.

iii. A gradual negative drift of the threshold voltage may shift the $V_{TH}$ of the device below a critical value. A too low threshold voltage can then cause parasitic turn-on during fast switching, thereby enhancing switching losses and device/module temperature.

To relax the first threat (i) one has to make sure that devices which see the same mission profile during application show a similarly narrow and predictable $V_{TH}$ drift. This is typically the case for intrinsic BTI. Problems only arise if the interface and gate oxide quality of individual devices show large variations, i.e. due to process inhomogeneity. Ionic contaminations within devices or packages may also degrade parallelization. However, as already mentioned previously, the effects of extrinsic BTI in Si and SiC technologies are similar and need to be prevented anyhow.

The second threat (ii) describes a degraded $R_{ON}$ due to a positive drift of the threshold voltage. In high power MOSFETs the $R_{ON}$ is typically a composition of essentially three major components

$$R_{ON} = R_{th} + R_{FET} + R_{PS}$$

(1)

In (1) $R_{th}$ is the channel resistance of the device, $R_{FET}$ is the
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