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An Efficient VLSI architecture design for logarithmic multiplication by using the improved operand decomposition

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ABSTRACT
Over the last few years, the Logarithmic Number System (LNS) has played a pivotal and decisive role in the field of Digital Signal Processing (DSP) and Image processing. Multiplication is a ubiquitous thirsty area to perform arithmetic operations in DSP applications and researchers have found that LNS is the possible solution for multiplication to be performed for a DSP application. In this paper, we propose a novel approach based on the Improved Operand Decomposition (IOD) to make an efficient logarithmic multiplier and subsequent the achievement through scale realization. The Pipeline technique and the efficient correction circuit are used for error minimization at the cost of minimal hardware and delay. Reported and proposed multiplier is evaluated and compared in terms of Data Arrival Time (DAT), area, power, Area Delay Product (ADP), and EPS (Energy per Sample) at 90 nm CMOS technology by using Synopsys design compiler. Simulation results show that the proposed IOD method for logarithmic multiplication without the pipelining gives maximum of 35.39 % less ADP and 11.15 % less EPS for 32-bit architecture than of the reported logarithmic multiplier architecture. The proposed IOD based logarithmic multiplier with the pipelining gives a maximum of 20.17 % less ADP for 8-bit architecture and 21.72 % for 32-bit architecture than of the reported iterative pipelined architecture of logarithmic multiplication. Simulation results show that the optimized logarithmic converter gives 7.32 %, and optimized antilogarithmic converter gives 41.59 % less ADP respectively than of the reported logarithmic and antilogarithmic converter structures. The optimized antilogarithmic converter architecture gives a maximum of 43.94 % less EPS than of the reported antilogarithmic converter structure.

Keywords-Divided approximation, FIR filter, Logarithmic, Logarithmic arithmetic, Mitchell method, Operand decomposition.

1. Introduction

Multiplication is an important component in DSP and Image Processing applications [1-4]. Especially, Finite Impulse Response (FIR), Fast Fourier Transform (FFT) and Discrete Cosine Transform (DCT) techniques need to be designed with an efficient multiplier [5]. But, as it is well-known fact that a multiplier has always been a limiting factor in terms of speed and large area. The LNS multiplier addresses to these issues and overcomes the burgeoning gap. LNS multipliers are advantageous over the Fixed Point (FXP) multipliers and Floating Point (FLP) multipliers to with their speed and accuracy [6-7]. LNS multiplier supports two families of native data-types: integer or fixed-point and floating-point number system. Fixed point multiplication is frequently used in general purpose digital processing applications due to the reason of easier algorithm, faster implementation, and a clear understanding. But, at the place where decimal
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