

Contents lists available at ScienceDirect

Microelectronic Engineering



journal homepage: www.elsevier.com/locate/mee

Research paper

Solid-state dewetting of single-crystal silicon on insulator: effect of annealing temperature and patch size



Marco Abbarchi^a, Meher Naffouti^{a,b}, Mario Lodari^c, Marco Salvalaglio^d, Rainer Backofen^d, Thomas Bottein^a, Axel Voigt^{d,e}, Thomas David^a, Jean-Benoît Claude^a, Mohammed Bouabdellaoui^a, Abdelmalek Benkouider^a, Ibtissem Fraj^b, Luc Favre^a, Antoine Ronda^a, Isabelle Berbezier^a, David Grosso^a, Monica Bollani^{c,*}

^a Aix Marseille Université CNRS Université de Toulon IM2NP UMR 7334, 13397 Marseille, France

^b Laboratoire de Micro-optoélectronique et Nanostructures Faculté des Sciences de Monastir Université de Monastir, 5019 Monastir, Tunisia

^c Istituto di Fotonica e Nanotecnologie Consiglio Nazionale delle Ricerche (IFN-CNR), L-NESS laboratory, via Anzani 42, 22100 Como, Italy

^d Institute of Scientific Computing, Technische Universität Dresden, 01062 Dresden, Germany

^e Dresden Center for Computational Materials Science (DCMS), Technische Universität Dresden, 01062 Dresden, Germany

ARTICLE INFO

Article history: Received 13 October 2017 Received in revised form 1 December 2017 Accepted 2 January 2018 Available online 03 January 2018

Keywords: Solid-state dewetting Nano-patterning Ultra-thin silicon on insulator

ABSTRACT

We address the solid state dewetting of ultra-thin and ultra-large patches of monocrystalline silicon on insulator. We show that the underlying instability of the thin Si film under annealing can be perfectly controlled to form monocrystalline, complex nanoarchitectures extending over several microns. These complex patterns are obtained guiding the dewetting fronts by etching ad-hoc patches prior to annealing. They can be reproduced over hundreds of repetitions extending over hundreds of microns. We discuss the effect of annealing temperature and patch size on the stability of the final result of dewetting showing that for simple patches (e.g. simple squares) the final outcome is stable and well reproducible at 720 °C and for ~1 μ m square size. Finally, we demonstrate that introducing additional features within squared patches (e.g. a hole within a square) stabilises the dewetting dynamic providing perfectly reproducible complex nanoarchitectures of 5 μ m size.

© 2018 Elsevier B.V. All rights reserved.

1. Introduction

In the race towards the miniaturization of photonic and electronic components, reliable fabrication methods of nanostructures play a strategic role in the reliable implementation of innovative devices. The use of silicon films on insulator (SOI) has a central position both in photonics (e.g. on-chip photonic circuits) and electronics (e.g. fully depleted SOI MOSFET) [1]. In these contexts, an important limiting factor towards the further reduction of the dimensionality of these components is the instability upon heating of ultra-thin SOI (UT-SOI, ~12 nm thick silicon on SiO₂) [2,3,4,5]. The presence of intrinsic defects in the thin silicon layer or of ad-hoc created edges (e.g. in order to define a device) are, upon annealing even well below the inherent melting temperature of the material, the starting points of mass transport in this phenomenon ruled by surface diffusion-limited kinetics of thermally-generated adatoms, known as solid-state dewetting [6].

During dewetting, under the action of surface diffusion, mass is accumulated in a thick, receding rim at the film edges (where the curvature of the film is large), which eventually becomes unstable and evolves in elongated structures (fingers). When other instabilities, such as corner

* Corresponding author. *E-mail address:* monica.bollani@ifn.cnr.it (M. Bollani). instability, bulging, rim pinch-off and faceting, take place the film breaks in isolated, monocrystalline, facetted islands [7]. The intricacies of these instabilities are further modified by the presence of preferential directions for mass transport, which must be taken into account in order to explain this complex dewetting scenario [8,9]. For example, it is well known that for a (001) oriented UT-SOI the dewetting speed along the [100] in-plane direction is much larger than that in the [110] direction [10]. These dewetting fronts are thus respectively called "unstable" and "stable". All these phenomena render de facto impossible the practical exploitation of UT-SOI for miniaturized devices.

The underlying dewetting instability, indeed, is characterized by a defined periodicity set by the initial film thickness h_0 . In real systems, however, thermal fluctuation and non-idealities (such as, e.g., the non-uniformity of the film thickness) actually make dewetting a rather disordered phenomenon and, at the end of the process, the spatial organization of the islands and their size dispersion are broadly distributed around their average values. This is an additional issue limiting the applicability of dewetted silicon films for instance, for applications in photonics [11,12].

In analogy with metals [20,21,22], a viable method for enhancing the level of ordering of the dewetted Si and SiGe structures relies on prepatterning the thin film prior to annealing [13,14,15,16]. Ordered arrays of complex islands arrangements can be obtained in a very limited set of configurations and on a limited number of repetitions by guiding the receding fronts through patches etched on the UT-SOI with a focused ion beam (FIB). This FIB-based method systematically leads to the formation of isolated (disconnected) monocrystalline islands limiting the control of the self-assembly and thus its applicability to more complex architectures. The fluctuation of the number of islands formed in a patch, their size, shape and position was between 4% and 35% [11]. More importantly, when using a FIB for etching, no receding rim was shown and the islands were always formed at the film edges at the early stages of dewetting [15]. These observations claim for spurious driving forces (e.g. ions implantation and amorphization during etching, re-crystallization during annealing) complicating the simple picture of pure surface diffusion limited-kinetics [17,18,19]. Alternative approaches based on e-beam lithography for creating small patches in the UT-SOI have been employed by several groups in the last years [20,21,22]. However, all these experimental results provided puzzling results suggesting that spurious phenomena in addition to pure surface-diffusion occurs, hindering the possibility to reproduce the results that Ye and Thompson showed for metal patches [23,24,25].

Here we show that with a proper annealing temperature and a suitable choice of pattern size and shape obtained by a combination of ebeam lithography and reactive ion etching processes, a well-controlled dewetting behaviour can be obtained also in semiconductors. We show that a perfect control of complex pattern shapes can be achieved for low annealing temperature (~720 °C) and by adding additional features within 5 µm large squared patches. Here we address the case of patches with sides oriented along the crystallographic axis [110] (the stable dewetting front). The case of patches oriented along the crystallographic axis [100] (the unstable dewetting front) is not taken into account here. In fact, in this condition, the patches rapidly undergo a fingering instability resulting in small, isolated and disordered islands [26]. Our findings fill the gap between semiconductors and thin films of metals [23,24,25] which dewetting features were expected to be general but never implemented so far in UT-SOI and opens the new possibility to exploit complex Si-based nanoarchitectures in electronic and photonic devices. Although not explicitly addressed here, it is worth mentioning that our results can be precisely reproduced by theoretical simulations based on a phase field modelling [27] providing a predictive tool for further engineering the final outcome of dewetting [16].

2. Experimental methods

An ultra-thin Si-on-insulator (UT-SOI) substrate (12 nm intrinsic Si film on 25 nm SiO₂ layer on Si(001) wafer) was patterned with a series of squares (depth ~12 nm, width of the etched squares between 0.5 µm and 5 µm) aligned along the [110] direction by means of e-beam lithography (EBL) and reactive ion etching (RIE). The resist has been spincoated on the Si substrate and then exposed to the electron beam of a converted scanning electron microscope (SEM) along the designed pattern (acceleration voltage of 30 kV). For these kinds of structures, a single layer of PMMA diluted to 2.5% and with a molecular weight of 950 k has been employed. The dose used for the structures was $300 \,\mu\text{C/cm}^2$. After the exposure, PMMA was then developed in order to remove the soluble exposed parts by a solution of methyl isobutyl ketone (MIBK) and isopropanol (IPA) in a 1:3 ratio. The MIBK was diluted in order to obtain well-defined profiles. The sample was immersed in this solution and agitated manually for 90 s: a pure IPA solution has been used for 1 min to stop the development of the resist. Then, the pattern was transferred to the thin Si film by reactive ion etching (RIE), using a CF₄ plasma, 50 WRF power and a total gas pressure of 5.4 mTorr. Finally, the resist was removed using acetone. The sample surface was then exposed to O₂ plasma in order to remove the residual resist. Additional chemical cleaning has been performed in N2 atmosphere before dewetting, by dipping the sample in a 5% HF solution for 20 s. EBL and RIE were performed following a well-established procedure schematized in Fig. 1a and the realized structures were characterized by SEM (Fig. 1b) and atomic force microscopy (AFM, Fig. 1c).

The etched patch shapes were simple squares (with side ranging from 500 nm up to 5 μ m) and large square patches (5 μ m) with additional features etched within them (e.g. holes, dashes, crosses, etc. Fig.1b and 1c). After etching, the samples were immersed in a 4% concentration aqueous HF solution for 5 s in a nitrogen atmosphere to eliminate any native oxide layer formed on top of the SOI. Thus, in the ultrahigh vacuum of a molecular beam reactor, the samples have been annealed at high temperature. All the investigated samples were cleaned with an annealing flash at 600 °C for 30 min in order to eliminate any trace of native oxide from the sample surface. Three different samples were annealed with different procedures: Sample A, @740 °C for 15'; sample B, @720 °C for 3 h; sample C, @ 800 °C for 1 h. The samples are characterized by different imaging techniques: AFM, SEM and optical dark-field microscopy (DF). During the DF analysis, the white light was shined with a ~70 degrees angle with respect to the sample surface. The light diffusion was collected by a high numerical aperture (NA = 0.75) 100× magnification objective lens and the images are registered with a colour-C-MOS camera [16]. As the overall collection angle in the NA of the objective lens was smaller than 70 degrees, the direct reflection from the sample was completely rejected and the flat surfaces appeared completely black. Note that the silicon islands were de facto dielectric Mie resonators, thus the collected signal was the resonant scattering from these nano-antennas. This was reflected in the different scattering colours visible in the DF images [11].

3. Results

We first address the effect of the annealing temperature on the final outcome of large and complex, squared patches (Fig. 2). A precise and reproducible ordering of the dewetted structures is only possible using annealing temperature below ~750 °C. In order to highlight this point, we analyse dark-field images of samples B (annealed at 720 °C for 3 h) and sample C (annealed for 800 °C for 1 h).

The bright scattering spots observed in dark field images correspond to individual islands. More precisely, provided that these objects are resonant antennas, different colours are attributed to resonant electromagnetic modes confined in each island [11,12,16]. These spectral resonances reflect their specific size, shape and composition and thus constitute a precise probe of the islands' homogeneity.

For low-temperature annealing we assist to the formation of a few large islands, eventually exhibiting multi-modal size distributions, with a rather good reproducibility of the complex arrangement over several repetitions (the overall patterns are 12×12 repetitions of the same patch design, not shown). Differently from the low temperature case, at high temperature the dewetting cannot be controlled and a random organization of many small islands is observed (Fig. 2 b). This feature reminds the typical results obtained via spontaneous dewetting of the same UT-SOI in non-patterned areas (not shown). In these experimental conditions (device thickness 12 nm and low annealing temperature, ~720 °C) the typical length of the underlying dewetting instability leads to isolated islands which are ~800 nm distant one from the other [11]. For the sake of thoroughness, we mention that temperature and patch orientation may influence this value [28].

Based on the previous results we investigate the impact of the overall dewetting time and of the patch size on the stability of simple, squared patches (without additional features etched within the squares) annealed at low temperature (samples A and B, Fig. 3). The relevant features are summarised as follows: 1) for short time annealing the process is not complete and the dewetting front moved of about 300 nm towards the center of the patch; 2) small protrusions start to form at the patch corners; 3) for longer annealing time the protrusion at the corners become more visible accounting for a reduced dewetting speed with respect to flat dewetting fronts along the patch edges; 4) for

دريافت فورى 🛶 متن كامل مقاله

- امکان دانلود نسخه تمام متن مقالات انگلیسی
 امکان دانلود نسخه ترجمه شده مقالات
 پذیرش سفارش ترجمه تخصصی
 امکان جستجو در آرشیو جامعی از صدها موضوع و هزاران مقاله
 امکان دانلود رایگان ۲ صفحه اول هر مقاله
 امکان پرداخت اینترنتی با کلیه کارت های عضو شتاب
 دانلود فوری مقاله پس از پرداخت آنلاین
 پشتیبانی کامل خرید با بهره مندی از سیستم هوشمند رهگیری سفارشات
- ISIArticles مرجع مقالات تخصصی ایران