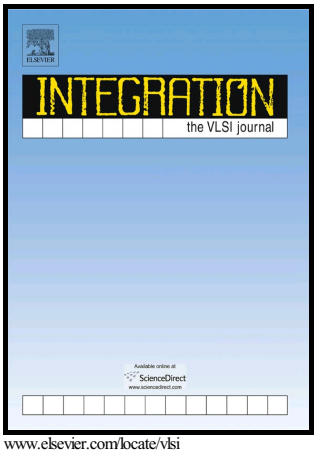

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RPF-DTT: Register Pre-allocation based Folded Discrete Tchebichef Transform (DTT) Architecture for Image compression

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Abstract— Recently, the large size data, power and real-time processing abilities are major issues in Digital Signal Processing/multimedia applications which require an adaptable architecture. The tool used for computing data decorrelation in the image processing applications refers Discrete Tchebichef Transform (DTT) which offers better performance than the DCT due to its bitstream coding capabilities. This paper proposes a novel model of Discrete Tchebichef Transform (DTT) architecture with Register Pre-allocation based Folded architecture (RPFA) for image compression. Through the cross-connection of folded architecture, the number of register usage is reduced. A Partial Cross Split Vedic Multiplier (PCSVM) method is introduced in the proposed DTT architecture. This multiplier design involves the cross function of the Vedic multiplier with the split pattern of multiplication binary stream. The optimal design of DTT architecture yields a minimum amount of FlipFlop (FF) counts, a latency and power consumption. The proposed PCSVM achieves higher Peak Signal to Noise Ratio (PSNR), better Structural Similarity Index (SSIM), lower delay, area, power consumption, Power-Delay Product (PDP), Mean Square Error (MSE) than the existing multiplier architectures. The proposed RPF-DTT architecture achieves a significant reduction in the resource consumption than the exact and approximate DTT architectures.

Keywords—Discrete Cosine Transform (DCT), Discrete Tchebichef Transform (DTT), Floating Point Processing Element (FPPE), Image Compression, Partial Cross Split Vedic Multiplier (PCSVM), Register Pre-allocation Folded Architecture (RPFA).

1. Introduction

Recently, the large size data, power and the real-time processing abilities are major issues in Digital Signal Processing/multimedia applications and the adaptable architecture is the immediate requirement to alleviate such issues. The performance of the entire system always depends on the top-level array interconnection and processing cell. The constructional issues of the top-level array and processing cell limit the throughput level adversely[1]. Hence, the extensible arithmetic processing elements are required to provide the guarantee to increase the throughput level. Based on the application requirements, the optimization and the prior knowledge are necessary during the design of processing elements such as registers, arithmetic units and control units. An orthogonal approximation of the Discrete Cosine Transform (DCT) is the major specification for the video and image processing applications. The good integer-based approximation of DCT coefficients plays the major role in the exact computation of transforms. The utilization of more number of registers for arithmetic operations and storage of results introduced the complexities in hardware design and huge power consumption. This paper focuses on the design of cross-connection of folded architecture to reduce the registers utilization in order to achieve less power consumption. High Efficiency Video Coding (HEVC) standard preceding the project called H.264/MPEG-4 AVC [2] specifies the definition of the semantic meaning of the syntax elements for the mapping of decoded pictures. The optimization of implementation process according to the application constraints and the prior knowledge regarding the implementation are the major requirements to meet the specifications of H.264/AVC. Discrete Cosine Transform (DCT) [3] and Just Noticeable Distortion (JND) [4] in H.264 have a major attention recently to adjust the quantization level to the threshold through the multiplication factor. The DCT also has the ability to support many video and image processing applications. An orthogonal approximation of 8-point DCT development in the research meet the specifications defined by the various image and video processing standards. The minimum complexity is the key characteristic in the combination of image compression with the quantization [5]. The good approximation of DCT coefficients plays the major role in the achievement of estimated results approached to the theoretical formulation. The integer-based approximations [6], [7], [8] act as an alternative approach for exact computation of the transforms. Real-time processing and the image transmission among the devices requires the suitable encoding algorithm with minimum complexity level. Listless Set partitioning embedded blocK (LSK) and Set Partitioning Embedded bloCK (SPECK) are considered as the low-complexity image encoding algorithms and they are simple to implement. The encoding of each insignificant band as zero increases the size of zeros in earlier passes and this leads to high-bit plane operation. An improved LSK (ILSK) algorithm coupled with the Discrete Tchebichef Transform [9] achieves the desirable properties such as reduction in length of bit string, time and memory consumption effectively. The number of registers utilization for multiplication and the storage of results are more in such DTT. This paper focuses on the design of cross-connection of folded architecture to reduce the registers utilization in order to achieve less power consumption.

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