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Enhanced transconductance in a double-gate graphene field-effect transistor

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ABSTRACT

Multi-gate transistors, such as double-gate, tri-gate and gate-all-around transistors are the most advanced Si transistor structure today. Here, a genuine double-gate transistor with a graphene channel is experimentally demonstrated. The top and bottom gates of the double-gate graphene field-effect transistor (DG GFET) are electrically connected so that the conductivity of the graphene channel can be modulated simultaneously by both the top and bottom gate. A single-gate graphene field-effect transistor (SG GFET) with only the top gate is also fabricated as a control device. For systematical analysis, the transfer characteristics of both GFETs were measured and compared. Whereas the maximum transconductance of the SG GFET was 17.1 μS/μm, that of the DG GFET was 25.7 μS/μm, which is approximately a 50% enhancement. The enhancement of the transconductance was reproduced and comprehensively explained by a physics-based compact model for GFETs. The investigation of the enhanced transfer characteristics of the DG GFET in this work shows the possibility of a multi-gate architecture for high-performance graphene transistor technology.

1. Introduction

Graphene has attracted considerable interest as a promising material for high-performance electronic devices due to its unique physical properties, such as atomically thin thickness [1], flexibility [2], high carrier mobility [3,4], and high thermal conductivity [5]. Due to the zero bandgap of graphene, the possible applications of graphene field-effect transistors (GFETs) are considered to be more suitable for high-frequency analog electronics [6–8], or detectors [9,10], rather than digital logic technology which requires a definite switching capability between an "on" and "off" state. One of the fundamental performance metrics of a FET is the controllability of the gate over the channel resistivity which is manifested as the transfer characteristics.

The transfer characteristics of GFETs have been extensively studied with a variety of structural considerations including a hexagonal boron nitride (hBN) substrate [11], a solution gate [12], a side gate [13], a high-quality gate dielectric layer [14] and a folded graphene channel [15]. Although it has been well-known in CMOS technology that a multi-gate structure, the mainstream of state-of-the-art nanoscale transistor design nowadays, greatly improves gate-to-channel control efficiency of a transistor [16,17], few studies have been done on the application of the multi-gate technique to GFETs. This raises the question of whether the advantage of a multi-gate structure that has been developed for several-nanometer-thick Silicon channel can still be effective for the one-atom-thick 2D channel. Furthermore, the previously reported double-gate structure of graphene transistors refers only to a metallic top gate and silicon substrate gate that act as two independent electrodes [18–22], not a pair of connected electrodes that applies an electric field symmetrically and simultaneously to both sides of the graphene channel. It should be noted that the aforementioned GFET is not a genuine double-gate structure but a quasi double-gate structure.

In this work, we report the fabrication of a double-gate graphene field-effect transistor (DG GFET) that is capable of modulating the graphene channel by the top and bottom gate simultaneously and symmetrically. The transfer characteristics of the fabricated DG GFET were compared to those of the single-gate graphene field-effect transistor (SG GFET) counterpart. The different characteristics between the SG and DG GFETs were further examined with a compact model for GFETs.

2. Experimental details

A highly doped (1–3 mΩ·cm) silicon wafer with a 90-nm-thick thermal SiO_2 was used as a substrate for the device fabrication. The bottom gate for the DG structure was patterned on a SiO_2 substrate with

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photolithography, and a Cr/Au (3/40 nm) stack was deposited with thermal evaporation. The bottom-gate dielectric film consists of a high-κ dielectric of 20-nm-thick Al_2O_3 film deposited by atomic layer deposition (ALD). Subsequently, a CVD-grown monolayer graphene was transferred onto the Al_2O_3 layer with polymethyl methacrylate (PMMA)-assisted wet-transfer method [23]. The graphene channel was defined by photolithography and followed by oxygen plasma etching for removal of the graphene outside the channel. The source and drain contacts were formed by evaporating Cr/Pd/Au (3/20/60 nm). An additional Al_2O_3 film that is identical to the bottom-gate dielectric was formed to act as the top-gate dielectric. Before the top-gate electrode deposition, in order for the top gate to be electrically connected to the bottom gate, a contact area was defined by photolithography, and the dielectric layer of Al_2O_3 inside the contact area were etched with dilute hydrofluoric acid. Finally, the top-gate electrode of Cr/Au (3/120 nm) was thermally evaporated to complete the device fabrication. As a control device, single-gate (SG) devices were also fabricated using the exact same procedure described above except for the bottom gate formation. DC electrical characterizations were carried out in a vacuum chamber (3 mTorr) at room temperature, with the Agilent 4156C Semiconductor Parameter Analyzer.

3. Results and discussion

Fig. 1(a) shows a cross-sectional schematic of the DG GFET developed in this work. The graphene channel is encapsulated by the Al_2O_3 dielectric layers at the top and bottom interface. The cross-sectional transmission electron microscopy (TEM) images of the DG GFET in Fig. 1(b) confirms that the double-gated structure and dielectric layers of Al_2O_3 were successfully fabricated as designed. The device used in this study had a gate length of 4 **µm** and a channel width of 6.5 **µm**. The gate underlap, which is the distance between the source/drain electrode and gate controlled region, was 2.3 **µm**.

Fig. 2(a) shows the transfer characteristics of the two different GFETs, one with a conventional single-gate (SG) structure (left) and the other with a double-gate (DG) structure (right). Drain current (I_d) is plotted as a function of the gate-to-source voltage (V_g) for fixed values of the drain-to-source voltage (V_d) increasing from 0.5 to 2.0 V. It is shown that the slope of the transfer curve is increased. Fig. 2(b) shows the output characteristics of a SG GFET (left) and a DG GFET (right). I_d is plotted as a function of V_d for fixed values of V_g-V_{Dirac} increasing from 0.85 to 5.85 V, where the V_g was chosen in such a way that the cross-over of I_d-V_d curves can be shown. The drain conductance of the DG GFET is slightly increased as well.

Typical graphene field-effect transistors exhibit ambipolar transfer characteristics with an electron conduction regime and hole conduction regime, and the regimes are demarcated by the minimum conductivity point [24]. The two regimes have their own maximum transconductance which is frequently used as a figure of merit for the current modulation of graphene FETs [2,11,14,15]. The fact that the maximum transconductance point occurs only once throughout the voltage sweep in each regime [14,25,26] makes the comparison of the maximum transconductances of the GFETs a useful method for performance evaluation. The transconductances, $g_m = dI_d/dV_g$, of the fabricated SG GFET (left) and DG GFET (right) are shown in Fig. 3(a), showing the apparent improvement by adopting the double-gate structure. Fig. 3(b) compares the maximum transconductance ($g_{m,\ max}$) between the SG and DG GFETs for a drain-to-source voltage of 0.5 and 2.0 V. The maximum transconductances were extracted from five different devices on the same wafer to examine possible device-to-device variations. At V_d = 0.5 V, the SG GFETs have an average $g_{m,\ max}$ of 17.1 **µS/µm**,

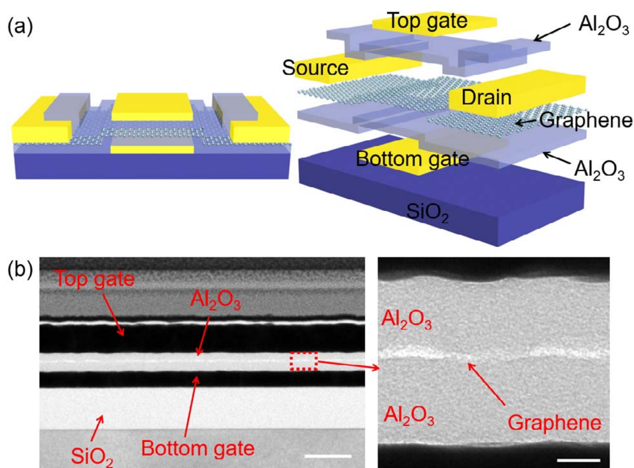

Fig. 1. (a) Cross-sectional schematic of the DG GFET used in this study. (b) Cross-sectional TEM images of the fabricated DG GFET. Monolayer graphene is in between the layers of Al_2O_3. Scale bar is 100 nm (left) and 10 nm (right).

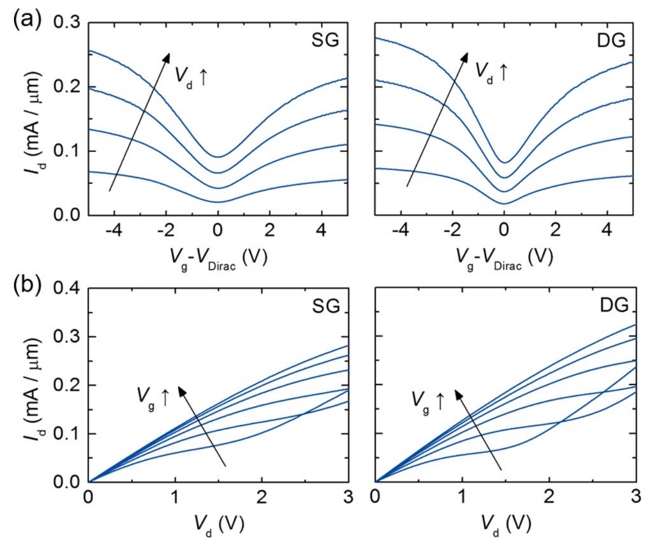

Fig. 2. (a) Transfer characteristics of a single-gate (SG) GFET (left) and a double-gate (DG) GFET (right). Drain current (I_d) is plotted as a function of the gate-to-source voltage (V_g) for fixed values of the drain-to-source voltage (V_d) increasing from 0.5 to 2.0 V. (b) Output characteristics of a SG GFET (left) and a DG GFET (right). I_d is plotted as a function of V_d for fixed values of V_g-V_{Dirac} increasing from 0.85 to 5.85 V. The devices have a gate length of 4 µm and a channel width of 6.5 µm.

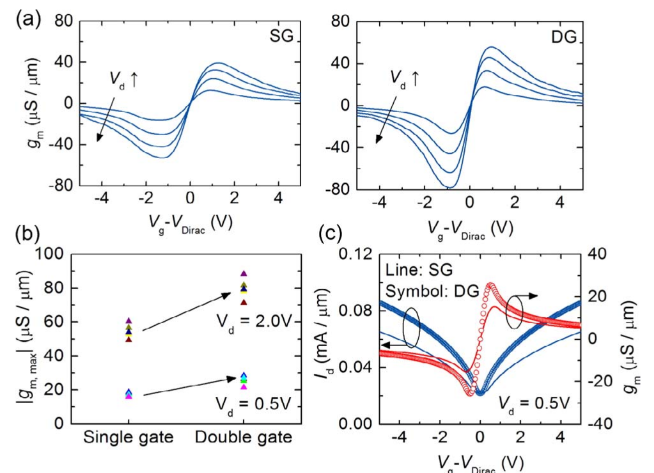

Fig. 3. (a) Transconductance (g_m) of the SG GFET (left) and the DG GFET (right). I_d is plotted as a function of the V_g for fixed V_d increasing from 0.5 to 2.0 V. (b) Comparison of the maximum g_m between SG and DG GFETs. Maximum g_m values were extracted from five different devices in the same wafer to check device-to-device variation. (c) Transfer characteristics and transconductances of SG (line) and DG (symbol) GFETs obtained with the compact model from [27] under V_d = 2.0 V.

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