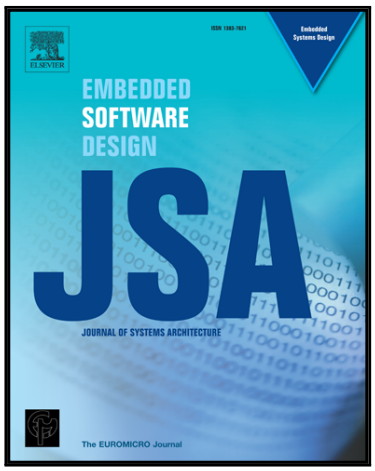

Efficient Task Spawning for Shared Memory and Message Passing in Many-core Architectures

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Efficient Task Spawning for Shared Memory and Message Passing in Many-core Architectures

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Abstract

Modern many-core systems consist of large number of processing cores and introduce more and more parallelism. The Partitioned Global Address Space (PGAS) programming model is a popular approach for exploiting this parallelism of architectures while offering flexibility of both shared memory and message passing paradigms. On the architecture design front, Network on Chips (NoCs) have become an integral part of the communication infrastructure due to their good scalability. In order to exploit task level parallelism on modern many-core architectures, the applications spawn more and more tasks to the available computing resources. The applications require less communication and synchronization delays for better performance. However, the distributed nature of NoCs poses a challenge to keep data communication and synchronization latency within the desired bound and hence results in higher task spawning overhead.

We proposed an approach based on hardware-assisted task spawning on many-core systems Zaib et al. (2015). In the current article, we present an extended version of our work for hardware-managed task spawning, keeping in view the communication requirements of both shared memory and message passing programming models. The proposed hardware support, integrated into the network interface architecture, reduces the synchronization

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