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Gate bias stress effect in single-walled carbon nanotubes field-effect-transistors

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ABSTRACT

This paper deals with the effect of negative gate bias stress with different times on the Carbon Nanotube Field Effect Transistor (CNTFET) based gas sensors, obtained using Single-Walled Carbon Nanotubes (SWCNTs) mats as channel. The effects of Gate Bias Stress (GBS) on transistor performance are important; hence it is necessary to understand how our device behaves under bias stress. To perform this work, I-V characteristics, are taken by applying a constant gate voltage (V_{gs}) for an extended time. I-V characteristics after stress exhibited an identical shape to the one before stress with an important degradation of the current that flows through the transistors. A possible source of the Bias Stress Effect (BSE) is traps in the semiconductor itself which are spatially and energetically isolated due to the disorder of SWCNTs. This hypothesis will be confirmed by the saturation of the drain current shift ΔI after a prolonged period of time. All isolated trap states are saturated and only electrical traps still active and give us the original I-V characteristics.

1. Introduction

The 20th century was the century of major changes in the electronics industry with the discovery of Carbon Nanotubes (CNT), by the Japanese researchers Sumio Ijima [1]. These cylindrical carbon molecules are one-dimensional molecular structures obtained by rolling up one graphene sheet to form a SWCNT or more than one sheet to obtain Multi-Walled Carbon Nanotube (MWCNT) [2]. Thanks to their small diameters around 1 nm to 4 nm, these long thin nanotubes can withstand incredibly high current rates and can be used as both metal wires and channels of Field Effect Transistors (FET). With these impressive mechanical [3], chemical [4], and electronic properties [5,6], SWCNTs can solve the problem of shrinking and building electronic devices [7], such as, CNT–FET based sensors [8]. The sensor technology based on SWCNTs has proven high sensitivity, high selectivity and low fabrication cost than other technology. However, many studies have reported that, developing stable and robust sensors based on SWCNTs as the functional material that can withstand ambient condition is challenging [9]. One fundamental parameter to be studied prior to practical application is the electrical stress [10] of the device in order to insure a stable device operation and to avoid device malfunction.

In this paper we report a detailed analysis of the behavior of I-V characteristics for different stress times and under ambient condition. We demonstrated that the shift of the I-V curves over time is associated to isolated traps in the semiconductor itself. The drain current shift ΔI became saturated after a short time, all isolated traps are saturated and we recovered back the original drain current after a natural relaxation without damage induced by the gate bias stress observed and without new traps created during GBS.

2. Experimental details

The device structure used in this work is shown in Fig. 1(b). Our device has been fabricated using n-doped Silicon substrates covered with 50 nm of thermally grown SiO_2. We have been prepared 16 couples of electrodes by UV photolithography: 4 pairs of each metal with inter-electrode distances of 10 μm and a width respectively of 1 and 3 mm, on (5 mm × 5 mm chip (see Fig. 1(a)). In this way we can modulate the final current value that flow between drain and source. The metal deposition has been performed using evaporation technique and lift-off, to obtain metal electrode thickness of 35 nm. A 5 nm Ti thick layer has been added in order to improve the layer adhesion of Au, Pd, Pt on the substrate.

The SWCNTs that we have used were CoMoCat SG65 composed by 90% of semiconducting SWCNTs [11] with a density of 1 $CNT/\mu m^2$. The SWCNT deposition has been achieved using a spray-gun technique

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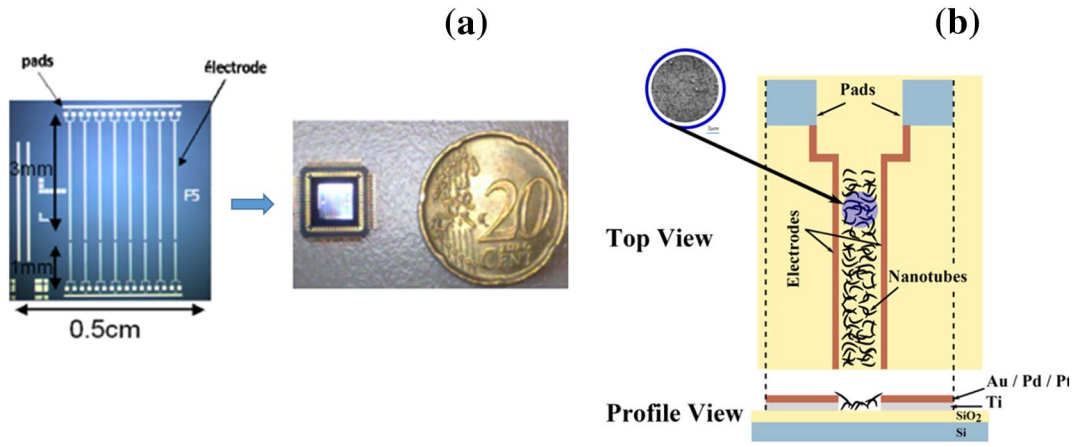

Fig. 1. (a) Chip dimensions for different metals as electrodes compared to a 20 cents coin. (b) Schematic view of one of the transistors. In the circle a SEM image of the SWCNTs.

which can be moved along the three axes (35 cm × 35 cm × 35 cm), to obtain uniform mats of nanotubes.

In order to analyze the effect of the BSE on I-V characteristics, current-voltage (I_{ds}-V_{ds}) measurements are taken using Keithely 2700, and LabView interface for data acquisition. The overall I-V characteristics including stress measurements are taken in the dark, at room temperature.

3. Results and discussions

3.1. I(V) measurements

The following metals were used for contacts—Pt, Pd, Au and Ti. The I-V characteristics of this device were determined and are presented in Fig. 2(a), respectively.

The transistors show different characteristics from one metal to another, identifying a sort of electronics fingerprinting. It is noted that the transistors obtained with Titanium electrodes have currents I_{DS} lower than those obtained with electrodes made of gold, palladium or platinum. The current in CNTFET is from the tunneling of carriers through the Schottky barriers. The type of metal for the contacts is chosen so that its work function ϕ_{SB} forces the metal Fermi Level to lie between the valance and conduction band of the SWCNTs.

At the intersection between the metal and the semiconducting SWCNTs, Schottky barriers are created. To understand the operation of a Schottky barrier, Fig. 2(b) illustrates the energy band diagrams situation of our CNTFETs which will be studied. Using a program developed in MATLAB, we notice that the metal with the highest work function gives the lowest Schottky barrier for holes. Pt, Pd, and Au have a high work function of (5.65 eV, 5.15 eV, and 5.1 eV) respectively, while Ti has a lower work function of 4.33 eV. This is expressed by currents evaluating in increasing order of work function in Fig. 2(a). These observations serve to highlight the essential role of the metal work function on the control of transistor performance [12]. We note that the use of variable metal work function can modulate the effective height of the Schottky barrier and thus to achieve an accurate measurement. In the following work we will focus our interest on the Ti electrode.

As can be seen from Fig. 3(a), the transistor is “On”, with a negative gate voltage (−1 V, −5 V). With a negative gate voltage applied, the Schottky barrier width at the source is modulated, allowing for holes to tunnel through the valence band and pass unblocked to the drain. This state is illustrated in Fig. 3(b). The thickness of the source Schottky barrier at the metal Fermi level decreases with an increasing gate voltage. Thus the tunneling current through the Schottky barrier increase, inversely to the barrier thickness.

If the gate voltage increases in the opposite direction, with a positive V_{gs}, the same effect will occur on the opposite side of SWCNT energy band, and the tunneling current through the Schottky barrier decreases. We switch to the “Off-state” as shown in Fig. 3(c). As a previous work confirmed that our semiconductor is P type [13], we can explain that the existing current on the off state (positive V_{gs}), is a combination between the strong memory of SWCNTs [14] and the leakage current that came from disconnected carbon nanotubes which can be modeled by a capacitance inactive with increasing positive gate voltage.

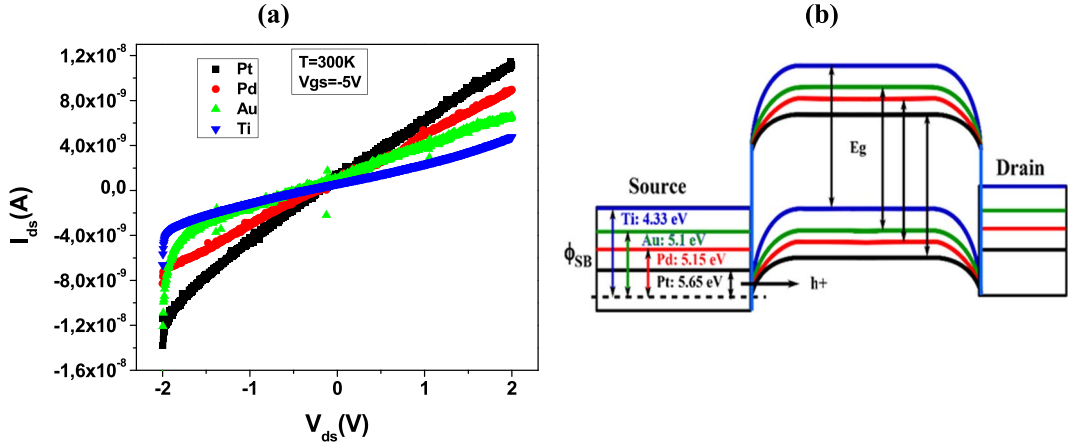

Fig. 2. (a) Measured I-V characteristics for different CNTFETs contacts with Pt, Pd, Au and Ti. (b) Schematic band diagram depicts the ϕ_{SB} differences using Pt, Pd, Au and Ti contacts, respectively.