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Effect of vacuum metalized gate electrode in top-gate solid-state electrolyte-gated organic transistors

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ABSTRACT

We report the effect of the metal-gate electrode in top-gate solid-state electrolyte-gated transistors (SEGTs). Here, a P(VDF-TrFE):P(VDF-HFP)-[EMIM][TFSI] dielectric blend is used as the solid-state electrolyte gate insulator (SEGI), with a variety of metal-gate electrodes, such as gold (Au), nickel (Ni), silver (Ag), and copper (Cu), and poly(3-hexylthiophene-2,5-diyl) (P3HT) as a semiconductor. Among the employed metal-gate electrodes, we achieved highest hole mobility of 3.26 ± 0.67 $cm^2V^{-1}s^{-1}$ in Au-gated P3HT SEGTs, which is ten times greater than the other metal-gated devices. The remarkable mobility in Au-gated devices is attributed to low contact resistance (Rc < 2 kΩ cm) and the exceptional electrochemical stability of the gold electrode. X-ray photoelectron spectroscopy (XPS) analysis reveals the formation of the oxide layers (NiO, Ni_2O_3, Cu_2O, Ag_xO) at the thermally-evaporated thin metal/SEGI interface. In a metal-insulator-semiconductor capacitor, the highly-conductive Ag and Cu based capacitors measured higher specific capacitance above 30 μFcm^{-2} compared to Au and Ni capacitors (~10 μFcm^{-2}) based on the same SEGI composition. Our findings provide useful insight for enhancing the charge injection and transport properties in top-gated electrolyte-gated transistors by selecting the appropriate top-gate metal electrode.

1. Introduction

Solution-processable high-capacitance solid electrolytes have been investigated to realize high charge carrier mobility, operational stability, and low operational voltage in field-effect transistors (FETs) [1–4]. Owing to the electric double layers (EDLs) formation in the electrolyte at the interfaces with the semiconductor and the gate electrode, electrolytes exhibit high capacitance values (> 1 μFcm^{-2}) compared to conventional dielectrics [5,6]. Demonstration of water [7–9], ionic liquids [10–12], ion gels [1,3,4], and polyelectrolytes [2,5,13] as a gate dielectric in organic FETs (OFETs) have been widely reported. However, the use of electrochemically stable and corrosion resistant materials, such as noble metals like gold (Au), platinum (Pt) or palladium (Pd) as the source, drain, and gate electrodes, are essential requirements for stable device performance. The gate electrode controls the charge concentration (channel conductivity) in the semiconductor film. The effect of different metal gate electrodes (Au, Pt, Cu, Ag, Ni, *etc*) has been investigated employing water, ionic liquid and polyelectrolytes gate insulators [7,8,12,13]. The gate electrode work function is an essential component which controls the threshold voltage (V_T) in conventional OFETs [14,15] and significantly in electrolyte-gated OFETs [7,8,12,13]. By employing a polyelectrolyte gate dielectric, Kergoat et al. demonstrated a direct impact of different metal-gate electrodes with various work functions (ϕ) in top gate electrolyte-gated OFETs [13]. A comparison of applied low ϕ calcium (Ca)-gate and high ϕ Au-gate showed a span threshold voltage over 0.7 V, revealing both depletion and enhancement modes in P3HT OFETs, and with a good correlation between the flat-band voltage and the threshold voltage using a variety of gate metal electrodes.

In this study, we report the effect of a gate-metal electrode in vacuum-deposited top-gated solid-state electrolyte-gated transistors employing various gate electrodes, such as Au, Ni, Cu, and Ag. Recently, we proposed and introduced a new polymeric solid-state electrolyte composed of a combination of high-*k* fluorinated polymer dielectric and an ion gel for high performance vacuum-metalized top-gate FETs [16]. This solid-state electrolyte gate insulators (SEGIs) showed high capacitance (> 1 μFcm^{-2}) ensuing from the combined polarization of -C-F interface dipoles and electrical-double-layer formation, and also allows for fabrication of evaporated thin metal top-gate electrolyte-gated devices. We engineered a number of SEGIs based on poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)): poly(vinylidene fluoride-*co*-hexafluoropropylene) and 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (P(VDF-HFP)-[EMIM][TFSI]) gel (Fig. 1a,b). XPS investigation showed oxide layers (NiO, Ni_2O_3, Cu_2O,

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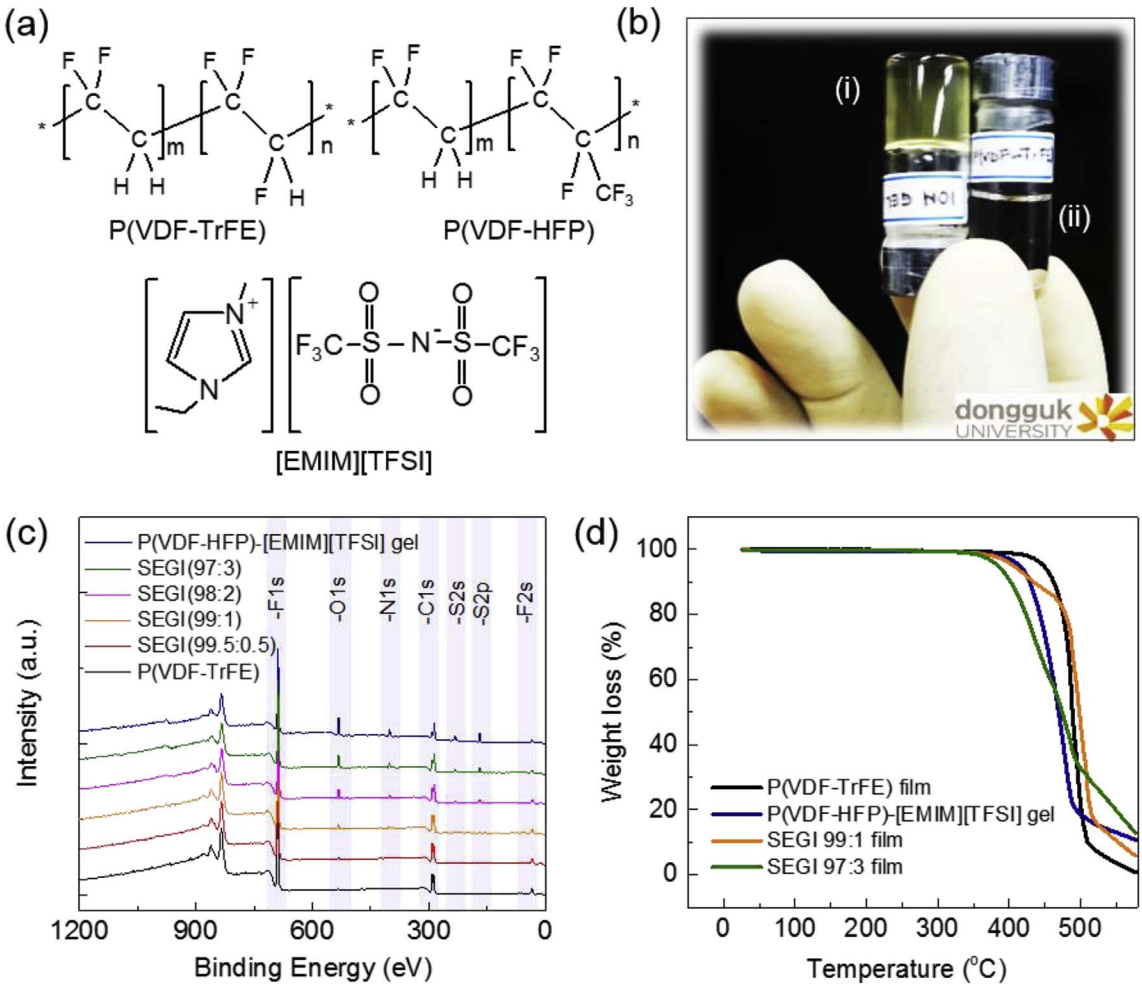

Fig. 1. (a) Molecular structures of the polymer dielectric blend containing the SEGI film: P(VDF-TrFE), [EMIM][TFSI], and P(VDF-HFP). (b) Photographic image of (i) P(VDF-HFP)-[EMIM][TFSI] gel and (ii) P(VDF-TrFE) solution. (c) X-ray photoelectron spectra of P(VDF-TrFE), indicated SEGIs and P(VDF-HFP)-[EMIM][TFSI] gel films. (d) TGA thermogram of P(VDF-HFP)-[EMIM][TFSI] gel, SEGI 97:3, SEGI 99:1, and P(VDF-TrFE) films, using a heating rate at 10 °C/min.

Ag_xO) at the vacuum-metalized SEGI interface. Among the employed metal-gate electrodes, Au-gated SEGTs recorded the highest mobility of 3.26 ± 0.67 $cm^2V^{-1}s^{-1}$. This mobility is ten times greater than the other metal-gated SEGT devices. The exceptional Au device performance is attributed to the low contact resistance (Rc < 2 kΩ cm) and better stability compared to the other metal-gates.

2. Experimental section

2.1. SEGT fabrication

The SEGT devices were fabricated using top-gate bottom-contact transistor architecture on conventional lift-off photolithography patterned Corning Eagle 2000 glass substrates (interdigitated source and drain electrodes (Au/Ni = 13/3 nm). The channel length (L) and width (W) are 10 μm and 1000 μm, respectively. The clean and oven-dried substrates are UV-ozone treated for 20 min. The P3HT (Rieke Metals, Inc) solution (10 $mgmL^{-1}$), was spun at 2000 rpm for 60 s ($d \approx 50.5$ nm) and thermally annealed at 150 °C for 30 min in a nitrogen-filled glove box. The P(VDF-HFP)-[EMIM][TFSI] gel solutions were prepared by co-dissolving P(VDF-HFP) (Mn = 130,000 $gmol^{-1}$ and Mw = 400,000 $gmol^{-1}$, Sigma-Aldrich) and [EMIM][TFSI] (HPLC, Sigma-Aldrich) in acetone, in a weight ratio of 1:4:7 and then heated at 70 °C for 24 h in a nitrogen atmosphere. Then, SEGIs were prepared by blending 0.5–3 vol% P(VDF-HFP)-[EMIM][TFSI] gel solution in 99.5–97 vol% P(VDF-TrFE) solution (30 $mgml^{-1}$ in 2-butanone) as in a previous publication [16]. The homogenously-mixed SEGI solution was then spin-coated (2000 rpm for 60 s) and thermally annealed at 80 °C for 1 h. 40-nm gold, nickel, silver, or copper as the gate electrode using a metal shadow mask was deposited by thermal evaporation at a rate of ~0.5 Å/s (without substrate heating) to complete the devices.

2.2. Thin film and device characterization

The atomic force microscopy (AFM) images of the metalized SEGI films surface microstructures were measured using non-contact mode AFM (Nanoscope, Veeco Instruments, Inc.). The field-emission scanning electron microscopy (FE-SEM) images were investigated using field emission-scanning electron microscope (FE-SEM; JSM-7100F). The metal work functions were measured by ultraviolet photoelectron spectroscopy (UPS; PHI 5000 VersaProbe II, ULVAC-PHI, Inc.). The chemical surface analyses of the SEGI layers (on SiO_2/Si substrates) were investigated by X-ray photoelectron spectroscopy (XPS; PHI 5000 VersaProbe II, ULVAC-PHI, Inc.). The sheet resistance of the deposited gate electrode (metal/SEGI) films were measured using the four-point probe method (RCHECK 4 point meter, EDTM). Average values from 7 to 10 measurements are reported. Capacitance characteristics were measured by a precision LCR meter (HP4284A, Agilent) and a semiconductor parameter analyzer (Keithley 4200-SCS). The effective surface area of the metal-insulator-semiconductor (MIS) structure is 0.0004 cm^2. The transistor electrical characteristics are measured by a semiconductor parameter analyzer (Keithley 4200-SCS). The mobility