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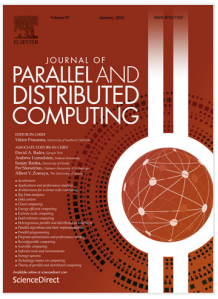

Caching architecture for flexible FPGA ray tracing platform

S. Collinson, O. Sinnen

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***Highlights (for review)**

* We investigate and propose an FPGA platform to efficiently explore ray tracing on FPGAs.

* We study the typical memory access patterns to the ray tracing data structures.

* We propose of a data structure specific cache and novel node cache replacement policy.

* Experimental evaluation of the proposed platform on real hardware is performed.

* The proposed cache architecture successfully alleviates the memory bandwidth bottleneck.

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