



A digital library for a flexible low-voltage organic thin-film transistor technology



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ARTICLE INFO

Article history:

Received 22 March 2017

Received in revised form

27 August 2017

Accepted 28 August 2017

Available online 1 September 2017

Keywords:

Organic thin-film transistors

Logic gates

Flip-flop

Shift register

ABSTRACT

This paper presents the design, fabrication and characterization of digital logic gates, flip-flops and shift registers based on low-voltage organic thin-film transistors (TFTs) on flexible plastic substrates. The organic transistors are based on the p-channel organic semiconductor dinaphtho[2,3-b:2',3'-f]thieno [3,2-b]thiophene (DNNT) and have channel lengths as short as 5 μm and gate-to-contact overlaps of 20 μm . The organic TFT is modeled which allows us to simulate different logic gate architectures prior to the fabrication process. In this study, the zero-VGS, biased-load and pseudo-CMOS logic families are investigated, where their static and dynamic operations are modeled and measured. The inverter and NAND gates use channel length of 5 μm and operate with a supply voltage of 3 V. Static and dynamic master-slave flip-flops based on biased-load and pseudo-CMOS logic are designed, fabricated and characterized. A new design for biased-load dynamic flip-flops is proposed, where transmission gate switches are implemented using only p-channel transistors. 1-stage shift registers based on the new design and fabricated using TFTs with a channel length of 20 μm operate with a maximum frequency of about 3 kHz.

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1. Introduction

Organic electronics paves the way for novel applications utilizing its compatibility with large-area and flexible substrates such as plastics, paper and fabric. Organic thin-film transistors (TFTs) have also been integrated with other technologies, such as ultra-thin silicon chips and printed sensors, in a hybrid system-in-foil (HySiF) [1,2]. In this system, the complementary advantages of the large-area and room-temperature-fabricated organic and printed electronics are combined with the high-performance silicon technology on a single flexible foil as a demonstration of a smart electronic skin for robotic applications.

Previous work has demonstrated the realization of organic-TFT-based complex circuits, such as shift registers (operating at frequencies as high as 10 kHz at a supply voltage of 20 V [3]), analog-

to-digital converters (signal-to-noise ratio of 26.5 dB [4]), digital-to-analog converters (resolution 6 bits and update rate 100 kS/s [5]), voltage generator (10 μA driving current), binary counter (14 bit) [6] and digital processors (40 instructions per second [?]). However, these circuits usually require high voltages to operate, which is a serious issue in mobile or wearable systems powered by small batteries. In this work, a digital library comprising basic combinational and sequential building blocks is developed, and circuits based on low-voltage organic TFTs are fabricated and characterized. A 1-stage shift register based on a new biased-load dynamic flip-flop design and fabricated using organic TFTs with a channel length of 20 μm operate with a maximum clock frequency of 3 kHz at a supply voltage of 2.2 V.

2. Fabrication

The organic TFTs and circuits are fabricated using high-resolution silicon stencil masks which provide a minimum resolution of a few microns [5,7]. The substrate is a stack of

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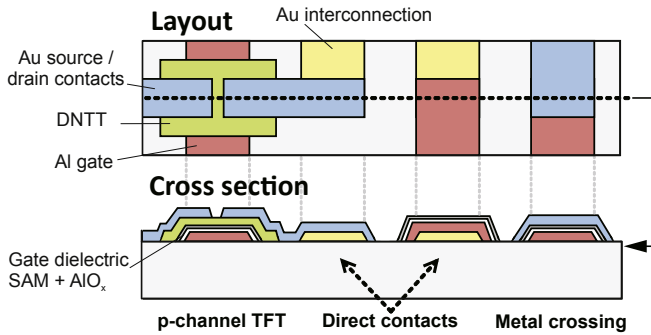


Fig. 1. Schematic showing the top and cross-sectional views of the inverted staggered (bottom-gate, top-contact) organic TFTs and the circuit interconnects. The gate electrode is aluminum (Al) and the source/drain contacts are gold (Au). The gate dielectric is a combination of AlO_x and an alkylphosphonic acid self-assembled monolayer (SAM). The organic semiconductor is dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNNT).

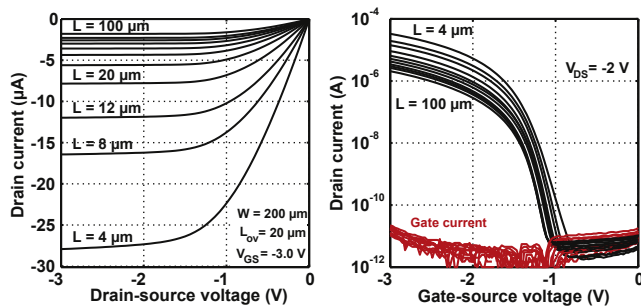


Fig. 2. Measured static output and transfer characteristics of organic TFTs with channel lengths (L) ranging from $100 \mu\text{m}$ to $4 \mu\text{m}$ fabricated on a flexible PI/BCB substrate. All TFTs have a channel width (W) of $200 \mu\text{m}$ and gate-contact-overlaps (L_{ov}) of $20 \mu\text{m}$.

Table 1
Extracted transistor parameters.

Parameter	Value
Threshold voltage V_{th}	-1 V
Mobility μ_0	$1.3 \text{ cm}^2/\text{Vs}$
Contact resistance R_c	$0.2 \text{ k}\Omega \text{ cm}$
Sheet resistance R_{sh}	$666 \text{ k}\Omega/\square$
On/off current ratio	10^6

polyimide (PI) and benzocyclobutene (BCB) with a total thickness of about $40\text{--}50 \mu\text{m}$ previously developed for a hybrid system-in-foil [1].

Fig. 1 shows the structure of the inverted staggered (bottom-gate, top-contact) organic TFTs. First, 30-nm -thick layers of gold and aluminum are deposited by thermal evaporation in vacuum through the first and second stencil masks to define the interconnects and the gate electrodes. The gate dielectric is a combination of a 3.6-nm -thick oxygen-plasma-grown AlO_x layer and a 1.7-nm -thick solution-processed tetradecylphosphonic acid self-assembled monolayer (SAM). The capacitance of the hybrid gate dielectric (C_i) is about 700 nFcm^{-2} [8] which allows the organic TFTs to operate at low supply voltages. A 25-nm -thick layer of the small-molecule organic semiconductor dinaphtho[2,3-b:2',3'-f]thieno [3,2-b]thiophene (DNNT) [9] is then deposited by sublimation in vacuum through the third mask. Finally, 25-nm -thick gold is deposited for the source/drain contacts through the fourth mask.

3. Organic TFT characterization and modeling

Fig. 2 shows the measured static output and transfer characteristics of organic TFTs with channel lengths ranging from $100 \mu\text{m}$ to $4 \mu\text{m}$ fabricated on the flexible PI/BCB substrate. The transmission line method (TLM) is used to extract the threshold voltage V_{th} , the intrinsic channel mobility μ_0 and the contact and sheet resistances R_c and R_{sh} [7,10]; the extracted values are summarized in Table 1.

In order to properly design an organic integrated circuit and simulate its behavior, a SPICE model is needed. Various organic TFT models have been proposed [7,11]. However, a model which is mature, fast, simple and suitable for circuit simulation with large number of TFTs was required in this work. The industry-standard Berkeley Short-channel IGFET Model (BSIM3) is chosen here to model the organic TFT behavior. Note that BSIM is used herein to model 4-terminal silicon-based transistors. However it is used here to model 3-terminal organic TFTs, which does not result in accurate or physical modeling rather than behavior modeling that is enough for organic TFT digital design. The measured static output and transfer characteristics of the TFTs are used to extract the device parameters. Fig. 3 shows the measurement data of our organic TFTs plotted against the simulated data using the BSIM3 model, showing good agreement between the measurements and the simple simulation model.

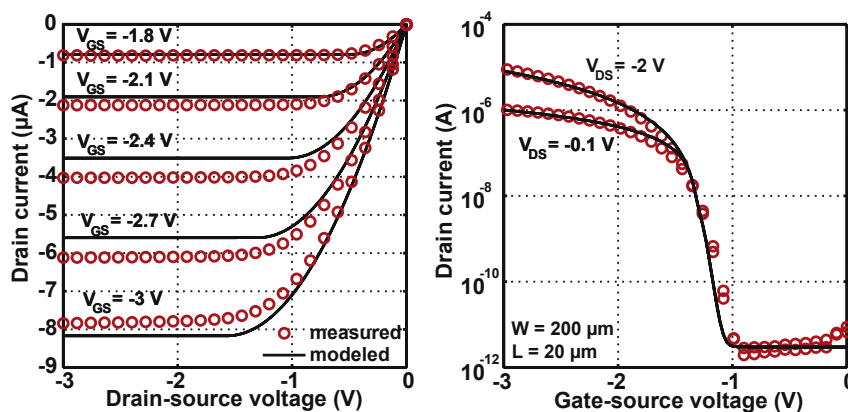


Fig. 3. Comparison of measured and modeled static output and transfer characteristics of an organic TFT with a channel length of $20 \mu\text{m}$.

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