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Solving the graphene electronics conundrum: High mobility and high on-off ratio in graphene nanopatterned transistors

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A B S T R A C T

Tens of graphene transistors with nanoperforated channels and different channel lengths were fabricated at the wafer scale. The nanoholes have a central diameter of 20 nm and a period of 100 nm, the lengths of the channel being of 1, 2, 4 or 8 μm. We have found that the mobility in these 2 μm-wide transistors varies from about 10400 cm^2/Vs for a channel length of 1 μm to about 550 cm^2/Vs for a channel length of 8 μm. Irrespective of the mobility value, in all transistors the on-off ratio is at least 10^3 at drain and gate voltages less than 2 V. The channel length-dependent mobility and conductance values indicate the onset of strong localization of charge carriers, whereas the high on-off ratio is due to bandgap opening by nanoperforations.

1. Introduction

Graphene electronics, which was still a hot topic few years ago, is loosing interest at the expense of two-dimensional (2D) materials electronics based on transitional metal dichalcogenides (TMDs) and X-nes (phosphorene, silicene, germanene). An updated state-of-the-art can be found in Ref. [1]. Graphene electronics was almost abandoned because the key electronic device – the graphene field-effect transistor (FET), cannot be switched on and off due to the absence of a bandgap. The lack of bandgap in the graphene monolayer has as dramatic consequence the suppression of saturation and blocking regions, the graphene monolayer FET (GFET) working as a voltage controlled resistance, but not as a switch. However, the mobility in graphene FETs attains impressive values, for example 23600 cm^2/Vs at room temperature in top-gated graphene nanoribbon FETs [2]. We have reported recently encapsulated GFETs with a nanoperforated channel, which show saturation and blocking regions tunable via the top gate voltage, and on/off ratios of at least 2×10^3 at room temperature at small drain and gate voltages, as well as a mobility of 2200 cm^2/Vs, higher than in many TMD monolayers such as MoS_2 or WS_2 [3]. Most TMDs show lower mobilities than Si, even as estimated from first principles [4], but excellent on/off ratios because they have a bandgap in the range of 1–2 eV. On the other hand, gapless X-nes, as graphene, show high mobilities, of 5200 cm^2/Vs, for example, in phosphorene FETs at room temperature [5], but are unstable in air, which is a huge drawback compared to graphene.

It is possible to solve the conundrum of graphene electronics: a GFET with a mobility having similar values as in graphene monolayer, or III-V semiconductor compounds based on GaAs or InP, and a high on-off ratio like in most 2D materials other than graphene or semiconductors? The issue is of huge practical importance, since a very high mobility is associated with a high-performance ultrafast transistor, i.e. an ultrafast switch. Such a switch could solve the main computer bottleneck, i.e. the stagnation of the clock speed of the computer CPU, which has not increased significantly since more than a decade.

We answer positively to the question before by showing that a GFET with a nanopatterned channel is in fact a high-mobility, high on-off ratio FET. Although the nanopatterning of graphene channels in GFETs was studied before, a careful perusing of the collection of papers mentioned in Ref. [3] and of the review [6] shows that previous results were based on unreliable lithographical methods, which lack on reproducibility. More precisely, the diameter of the holes, the distances between them and in some cases even the patterned are difficult to be preserve on large areas. Therefore, no transconductance or mobility values in these structures were reported before, despite the fact that the first attempts to fabricate nanopatterned GFETs are seven years old [7]. On the other hand, batch fabrication of nanopatterned FETs and their encapsulation [3] resulted in high transconductance, mobility twice as large as in Si, and high on-off ratio. In this paper, we extend our analysis of nanopatterned GFETs in Ref. [3] by scaling down their dimensions and performing a batch fabrication based on e-beam lithography of 90 nanopatterned GFETs with channel lengths of 1, 2, 4 and 8 μm. The aim is to study the dependence on the channel length of mobility, drain conductance and on-off ratio,

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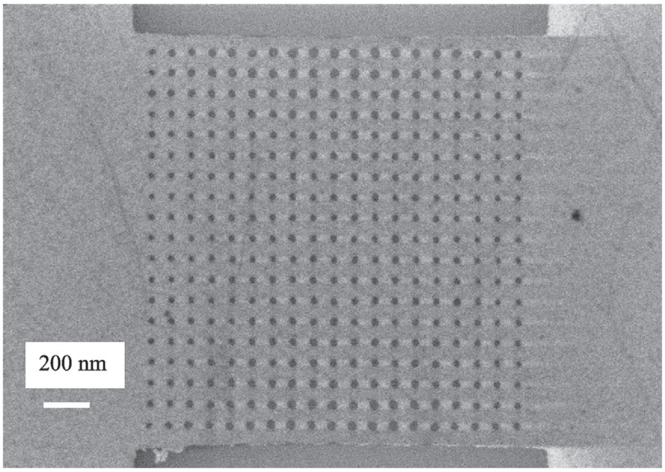

Fig. 1. SEM image of a nanopatterned GFET channel with $L = 2$ μm.

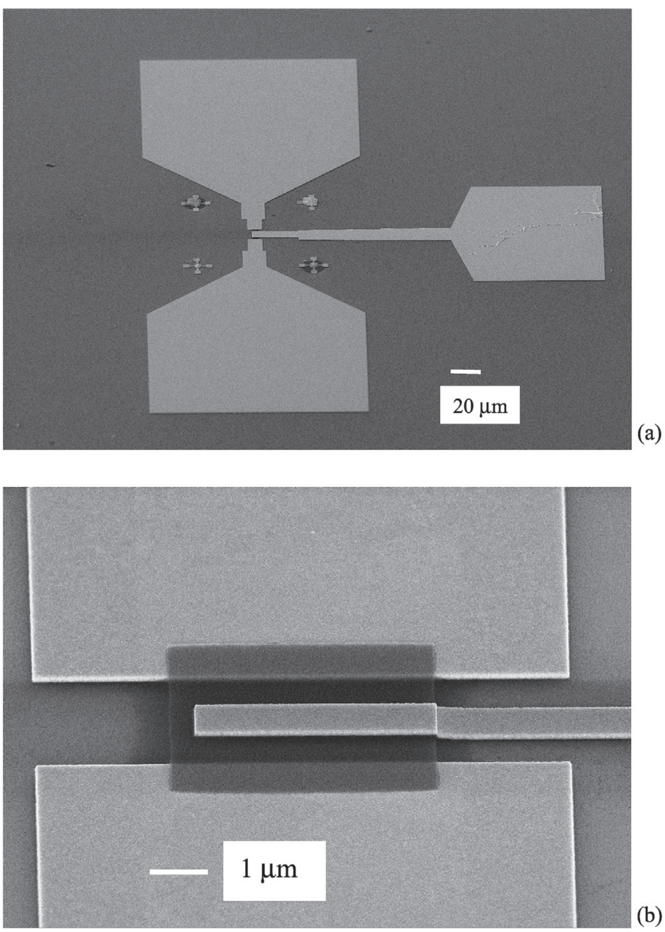

Fig. 2. SEM images of (a) the nanopatterned GFET, and (b) a corresponding detail of the source-drain region.

and to elucidate the transport phenomena in these GFETs. We have found that (i) the mobility decreases from 10400 cm^2/Vs for the GFETs with 1 μm channel up to 550 cm^2/Vs for a channel length of 8 μm, indicating that strong localization of carriers takes place in GFETs, with an average localization length of 1.9 μm, and that (ii) the on-off ratio is higher than 10^3 in all transistors at drain and gate voltages less than 2 V due to the bandgap induced by nanopatterning.

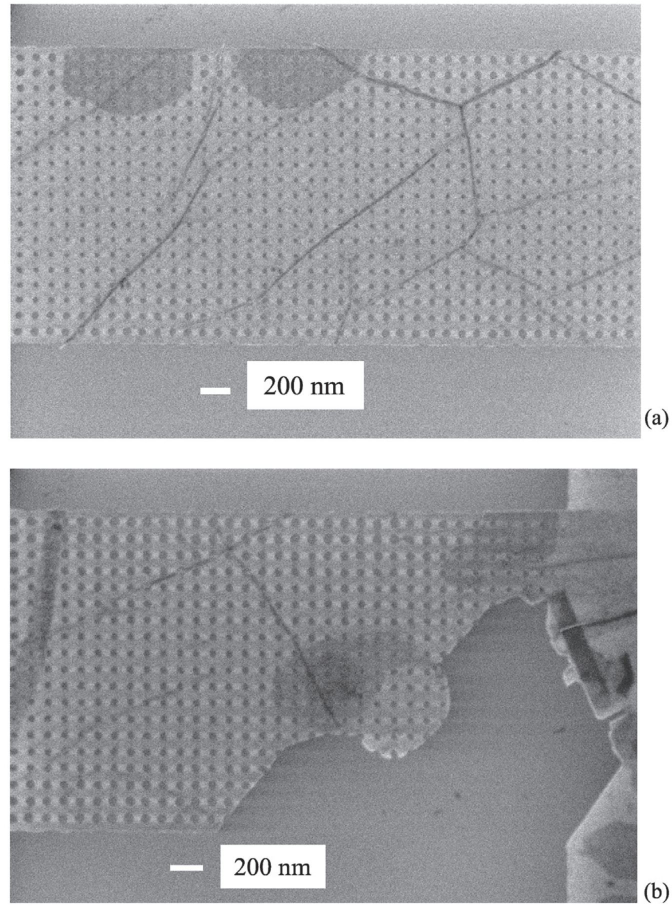

Fig. 3. Defects in a GFET channel: (a) multiple cracks accompanied by resist debris, and (b) ripped graphene flakes.

2. Fabrication and characterization of nanopatterned GFETs

The graphene monolayer, grown by the CVD method, was transferred on a 4 inch Si/SO_2 substrate. The SiO_2 layer has a thickness of 300 nm and the Si substrate has high resistivity, greater than 8 kΩ cm. Raman analysis was used to verify the graphene quality transfer and the persistence of graphene monolayer characteristic after certain critical fabrication processes involving especially PMMA removal and dielectric deposition. Raman analysis, performed on different areas of the wafer, show that the transferred CVD-grown graphene monolayers form in fact islands with maximum dimensions of 5 mm. These monolayer islands are surrounded and connected by a network of wrinkles, where all types of graphene, from bilayers up to multilayers, can be identified. In all tests, we considered that graphene monolayers preserve their properties if the D band is absent, if the G band has a peak around 1586 cm^{-1} and the 2D peak is around 2640 cm^{-1}, and if the ratio between the 2D and G peaks is at least 2. The result was that we found mainly graphene monolayers in a large region, of about 40% of the wafer. Although the Raman map of the wafer is time consuming, it is necessary in order to make sure that the selected region has a smaller number of defects than the surrounding regions.

Further, we have cut the selected graphene chip from the wafer and started the fabrication process for 90 GFETs with nanopatterned channels. We have fabricated nanoperforated GFETs with channel lengths of $L = 1$, 2, 4 and 8 μm. Twelve steps are necessary for batch fabrication of nanopatterned GFET. First, the graphene channels of all 90 GFETs are fabricated via e-beam patterning and reactive-ion etching, followed by nanoperforation by e-beam. The nanopatterning consists of a periodic array of holes, with a diameter of 20 nm and a period of at 100 nm,