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Study of silicon chip soldering in high-power transistor housing

Vasily S. Anosov, Denis V. Gomzikov, Maxim I. Ichetovkin, Lev A. Seidman*, Roman I. Tychkin

GZ Pulsar JSC, 27 Okruzhnoy Proezd, Moscow 105187, Russia

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ABSTRACT

The aim of this work is to study the possibility of reducing the labor consumption and cost of high-power silicon transistor manufacturing without compromise in transistor low thermal resistance. To this end we experimentally explored replacing Au-Si solder with lead-silver solder or other solders for silicon chip soldering in transistor housings. This will reduce gold consumption and increase the efficiency of high-power transistor silicon chip installation due to the use of batch soldering technology. We also studied the effect of different silicon wafer back side treatment and thinning methods on the thermal resistance of the transistors. To improve the soldering quality we applied preliminary Ti–Ni metallization of the reverse side of the silicon wafer.

We experimentally assessed the effect of outer housing layer materials and back side chip metallization. For lead-silver soldering of silicon chips, the best housing is that with a nickel outer layer rather than with a gold-plated one, because the resultant thermal resistance is lower and the absence of gold makes the technology cheaper. We obtained a 0.6 K/W thermal resistance for a 24 mm^2 chip area.

Introduction

The quality of transistor chip installation in transistor housing is characterized by the thermal resistance of the assembled transistor. Achieving the lowest possible thermal resistance is of utmost importance for high-power silicon transistors. There are several high-power silicon transistors chip soldering methods including those with gold-silicon eutectic solder [1], lead solder [2] or lead-free solder e.g. gold-tin alloy [3–6].

Commercial high-power silicon transistors, e.g. KT-866, are soldered with gold-silicon eutectic forming as a result of gold interaction with the back side of the silicon chip.

The aim of this work is to study the possibility of reducing the labor consumption and cost of high-power silicon transistor manufacturing without a compromise in the low thermal resistance of the transistors. To this end we experimentally explored the replacement of Au–Si solder with lead-silver solder or solder pastes for silicon chip soldering in the transistor housing. This will reduce gold consumption and increase the efficiency of high-power transistor silicon chip installation due to the use of a batch soldering technology.

Experimental

We experimentally studied the installation of KT-866 high-power transistor 6 × 4 mm^2 chips in KT-57 housings. The commercial KT-866 transistor technology uses 450 μm thick ∅76 mm *n*-type conductivity raw silicon chips with epitaxial layers on the polished working surfaces. Transistor structure fabrication and sorting are followed by chip thinning for thermal resistance reduction by mechanical grinding to a 260 μm thickness and chip back side polishing to an approx. 15 μm depth. The transistor chips are installed in the housings manually by vibration soldering with gold-silicon eutectic solder on a gold pad, using an EM-4075A periodic action instrument. The average thermal resistance of commercial KT-866 transistors is 0.66 K/W. The thermal resistance tolerance for the device is 1.0 K/W as per the standard.

Wafer polishing is required after grinding due to a specific problem faced during gold-silicon eutectic soldering of ground thinned chips. The wafer surface has visible linear roughness (scratches) with depths of several micrometers produced by grinding (Fig. 1). Moreover, there is a damaged layer with a thickness of approx. 1–2 μm (Fig. 2) [7]. The effective surface area of the chips is therefore several times greater than their geometric area. Therefore the quantity of silicon oxide on the surface is greater than expected, and the effective interaction area of the gold solder pad and the silicon chip is smaller than the contact area. As a result the thermal resistance of the chip/solder interface increases. Thus, to obtain a smooth surface the technology includes mechanical polishing of the silicon chip back side or etching in acids (HF or HNO_3) on a centrifuge [7]. This method allows removing a 10–30 μm layer [7]. The above operations increase the labor consumption and cost of the transistor technology.

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* Corresponding author.
E-mail addresses: seid1@yandex.ru (L.A. Seidman), kb-it@mail.ru (R.I. Tychkin).

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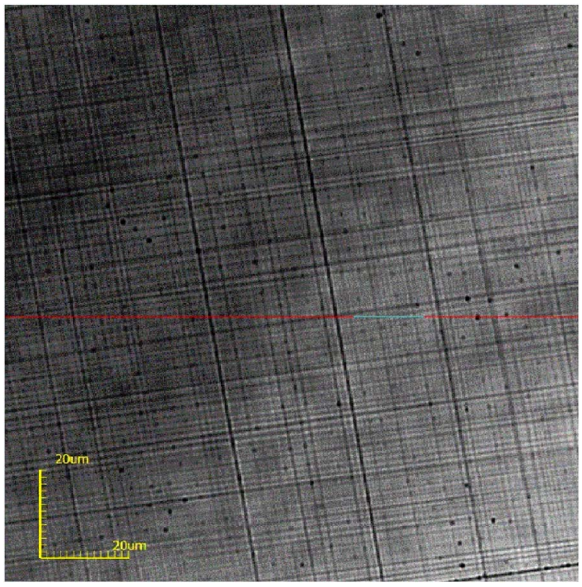

Fig. 1. Roughness after silicon chip back side grinding.

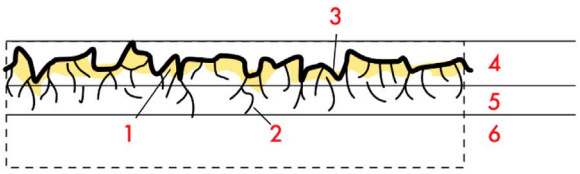

Fig. 2. Cross section of ground wafer: (1) inelastic strain area, (2) microcracks, (3) As-ground surface, (4) 0.5–1.0 μm roughness layer, (5) 1.0–2.0 μm subsurface layer, (6) bulk [7].

Unlike earlier [7] we did not mechanically or chemically polish the ground wafer; instead we only treated its back side as follows:

– deep grinding (to 260 μm) for chip thinning;
– shallow grinding (to 8 μm) for removing the damaged and contaminated silicon layer.

Following this we applied metallization on the back chip surface. Metallization is required since non-metallized silicon surface has very low lead-silver solder acceptance. The thermal resistance data for the transistors will be discussed below and compared with the data for the commercial KT-866 device manufacture process.

Equipment

The back sides of the silicon chips were ground on a high-output EM-2050 grinding machine. The standard as-ground chip rinsing process combined fluid rinsing and ultrasonic treatment.

After grinding and rinsing we coated the wafer back sides with two-layer Ti–Ni metallization (0.1/0.1 μm) in a single process on a Kurt J. Lesker PVD 250 plant [1,2]. Metallization is required since non-metallized silicon chips have very low lead-silver solder acceptance. We did not heat the wafers during metallization. The metal was electron beam evaporated from tungsten crucibles. The wafers were argon beam bombarded for 5 min. in the vacuum chamber before titanium sputtering for silicon oxide layer removal and improving titanium film adhesion aimed at producing an adhesive sublayer. The overlaying nickel film is required for providing a well-wetted non-oxidized surface. Furthermore, the advantage of nickel for lead-containing solders is the absence of transition phases in the Ni–Pb system and the almost perfect mutual insolubility of the two metals at up to 600 °C even if lead is liquid [8].

The silicon wafer was diced on a proVectus ADT (advanced dicing technologies) 7100 dicing device.

Soldering operations with various solders were conducted in an SST-5100 programmable furnace. SST-5100 is a vacuum furnace having pumping, injection, blowing and suction functions at pressures of $\sim 7{\cdot}10^{-5}$ to 2.7 atm. The furnace software allows varying the temperature of the pieces, aging and pressure decrease / increase at any time in the course of an automatic processing cycle. This vacuum furnace allows soldering of 100 KT-57 housings simultaneously in only 30 min. including the housing loading and unloading time. Hereinafter we will consider the soldering temperature as the platform temperature in the furnace chamber which is a priori higher than the temperatures of the device housing, the solder and the chip, because the heat flow passes from the platform to the solder and the crystal via the housing, this process being dependent on the heat conductivity of the above-mentioned components and the heat contact resistance between them. There is a parallel heat flow from the platform to the device housing, the solder and the chip via formiergas if the latter is used for soldering.

We used a 3600 single-head ultrasonic wedge bonding system for micro-bonding of contacts.

The wafer surface morphology and transistor appearance were examined under an OLS40003D measuring laser microscope. Direct thermal resistance measurement of the soldered contacts was carried out on a BKVP411189044 device developed by Pulsar JSC.

Experimental

The experiments included soldering of KT-866 devices into gold- or nickel-plated KT-57 housings with different solders. We used back side metalized chips diced from three types of silicon wafers differing in back side mechanical treatment degree:

1. Wafers ground thinned to 260 μm.
2. Shallow thinned wafers (~ 8 μm).
3. Raw wafers without back side grinding.

The solder was in most experiments a 100 μm thick lead-silver solder preform consisting of 2.5% Ag + 92.5% Pb + 5% Sn [9]. By way of comparison was also used Indium Corporation solder pastes, i.e. Indium NC-SMQ®75 paste having the same composition as the solder preform and Indalloy 182 paste of the Au 80% + Sn 20% composition. The melting points of the solders are close, i.e. 295–300 °C for the lead-silver solder [9] and slightly lower for the gold-tin alloy, 280 °C [3,5,6]. The soldering temperatures (the highest platform temperature in the furnace chamber) were in all the experiments significantly higher than the solder melting point. In some soldering processes we used Indium TACFlux 010 flux gel [10] applying it in a thin layer on the device housing and on the solder preform.

We used two soldering modes:

– Mode 1: at 350 °C in working gas atmosphere under flux [2];
– Mode 2 (alternative): at 350–450 °C in vacuum without flux.

A distinctive feature of the second (alternative) furnace automatic cycle operation mode was that most of the working cycle was conducted in vacuum which was developed before solder melting, unlike conventional soldering modes [11,12] for which furnace vacuum is developed during soldering when the solder is already liquid. A significant disadvantage of the conventional process is that the gas cannot be completely removed from all the cavities formed by the surface roughness of the soldered pieces because the melt covers the cavities separating them from the rest of the vacuum chamber space [13–15]. We therefore developed vacuum in the furnace at the preparation stage when the solder was still solid and there were channels between the solder and the chip for efficient gas removal. For our experimental setup there was no gas in the cavities which could hinder cavity filling

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