Microprocessors and Microsystems 000 (2016) 1–14

Contents lists available at ScienceDirect

Microprocessors and Microsystems

journal homepage: www.elsevier.com/locate/micpro

Odd/Even Invert coding for phase change memory with thermal crosstalk

Imtiaz Ahmad, Areej Hamouda, Mohammad Gh. Alfailakawi*

Department of Computer Engineering, Kuwait University, Kuwait

ARTICLE INFO

Article history:
Received 10 March 2016
Revised 18 July 2016
Accepted 30 November 2016
Available online xxx

Keywords:
Phase-change memory
Memory write performance
Lifetime
Write endurance
Coding

ABSTRACT

Cloud based services demand a colossal amount of memory in order to satisfy their objectives. Phase-change memory (PCM) has emerged as one of the most promising memory technologies to feature in next generation memory systems. One of the key challenges of PCM is the limited number of writes that can be performed on memory cells also known as "write endurance". In this paper we present a cost model which captures the asymmetry as well as disturb characteristics associated with write operations in PCMs. Moreover, we present an encoding architecture based on the proposed cost metric to allow the write operation to be performed using minimum cost. The proposed approach called "Odd/Even Invert" re-codes data based on selective inversion of even and/or odd bits to find minimum cost write operation that shall enhance cells lifetime. The proposed approach inquires a cost of only two extra bits regardless of the size of data word used, hence provides a cost effective approach to the problem. Experimental results and comparison with existing techniques on random data, real data, and memory traces from PERSEC benchmark suite, show the effectiveness and scalability of the proposed scheme.

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1. Introduction

Memory has been the key component of computer systems right from the beginning. The convergence of consumer, communication, and data processing applications combined with the rapid growth of cloud computing services have led to an explosive growth in memory requirement [1,2]. At present, DRAM and NAND flash memories together make up 89% of the memory market [1]. The success of DRAM and flash has been essentially attributed to their small cell size and scalability. To meet the ever-growing demand for modern multi-core systems to process data at higher rates, there exist serious challenges that shall limit the dominance of DRAM and flash memories. The unavailability of cost effective scalable lithography for sub-20 nm feature size is one of the factors affecting further evolution of such memories [3]. These challenges have spurred great interest in alternative technologies to shape the landscape of future memory systems. Among the competing contenders, phase-change memory (PCM) has emerged as one of the most promising memory technologies for the next generation memory systems due to its salient features of high density, superior scalability, very low leakage power, low latency, good endurance, long retention (over 10 years), large capacity, byte addressability, shock-resistivity and better reliability compared to other non-volatile memories [4–7].

PCM has better write endurance than flash memory, thus complicated wear-leveling circuitry commonly needed in flash-based systems is eliminated. Further, unlike flash memories where an erase operation is performed on a block, PCM write operations can be programmed at bit level with faster speed without the need for block erasure. In addition, PCM requires a lower mask overhead than flash, thereby reducing manufacturing costs for embedded applications. Moreover, PCM integrates well with traditional CMOS processes allowing easy migration to new technologies. Lastly, PCM technology potentially surpasses the scalability of DRAM as well as NAND flash memories [8–11]. Given these advantages, PCM is poised to deliver low cost, easy to manage, high-speed unified memory to usher in the next generation of non-volatile memory solutions [4–12].

PCM is a resistive non-volatile memory that use phase changing properties of chalcogenide alloy (Germanium-Antimony-Tellurium: $Ge_2Sb_2Te_2$), commonly called GST, to store information by reversibly switching between two states with completely different resistances: high resistance amorphous state that stores value "0", and low resistance crystalline state that stores value "1" [13,14]. Writing a "0" is commonly referred to as a Reset operation in PCM terminology whereas writing logic "1" is known as a Set. To Reset a cell, a large current is injected into the cell resulting in high temperature that melts the GST material. Then, the current is abruptly

* Corresponding author. Fax: +96524839461.
E-mail address: alfailakawi.m@ku.edu.kw (M.Gh. Alfailakawi).

http://dx.doi.org/10.1016/j.micpro.2016.11.015
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removed hence quenching the GST into amorphous state. For the Set operation, the current pulse is smaller in magnitude but longer in duration. Therefore, the GST is heated to a temperature between melting and crystallization thus allowing the chalcogenide material to crystalize.

Despite all the advantages of PCM, it exhibits several challenges associated with the write operation such as limited endurance, high energy, and long latency [12,14,15,16]. With respect to cell lifetime and endurance, a typical maximum number of write operations to a PCM cell is limited to 10^9 write cycles. Even though better than flash, such write endurance characteristic is not sufficient when compared to DRAM memory which have infinite lifetime. In addition, PCM shows asymmetry with respect to the Set and Reset operations [15–18] where Reset consumes higher power than Set, while Set takes longer time. This asymmetrical behavior is ignored by many write schemes such as [19–26], since such approaches assume that writing a bit consumes the same power regardless of the value being written, thus limiting bit write parallelism. Moreover, in such schemes, writing a bit is considered to take an equal amount of time regardless of the value to be written, which is not true, hence can increase write command latency.

The limited write endurance of PCM hinders its widespread usage in computers and embedded systems [12]. Therefore, enhancing PCM lifetime is of great importance especially if is to replace DRAMs in the future. The endurance problem in PCM can be addressed by reducing the number of bits written while serving write requests. Such practice would decelerate the wear out rate and will increase cell lifetime. Consequently, several techniques have been proposed to reduce the number of written bits when servicing writes [16,19–26]. Most of the reported bit-write reduction techniques do not take into consideration write asymmetry and treat bit values of zeros and ones equally. As it was mentioned earlier, writing a “0” takes more current and generate heat above melting temperature which will wear out the cell quickly. Therefore, writing a “0” is more detrimental to cell endurance than writing a “1” [27,28]. Moreover, writing a “0” may give rise to write disturb problem in PCM due to inter-cell thermal crosstalk during programming [29–32]. Write disturbs alter the content of memory cells while operating on others, thus resulting in errors in stored data. Therefore, focusing only on reducing the number of bit flips in write operations does not capture all dimensions affecting the endurance and bit error rate in PCM.

Although the asymmetry of the Reset and Set operation have been considered by some authors for various PCM optimization [17,18,33,34], the authors in [35] has recently introduced CAFO, a simple and an elegant cost model that captures such asymmetry. Based on their cost model, the authors proposed an encoding scheme that is capable of reducing overall cost of write operations. Even though, the decoding process is simple, CAFO's encoding process is complex and incur a computational overhead on cells write path. Moreover, most of the reported techniques, including those that consider the asymmetry of the write operation such as CAFO [35], do not take into consideration the thermal crosstalk or write disturb in their cost models.

In this paper, we propose a write reduction mechanism, called *Odd/Even Invert* to improve PCM lifetime. We modified the cost model developed in [35] to include more encoding options and incorporated the effect of write disturbs into the proposed model. The encoding/decoding process proposed is very simple but very effective and is based on selective bit inversion (odd, even, full). The proposed encoding scheme is discussed and presented both at algorithmic as well as architectural level, and it can be easily integrated with existing techniques. Simulation results shows the effectiveness and the scalability of the proposed approach when compared to previously proposed ones. According to best of our knowledge, the proposed approach is the first technique addressing both bit flips and write disturbs caused by thermal crosstalk at the same time as a mean to extend PCM lifetime.

The paper is organized in the following manner: In Section 2, we review basics of PCM memories and present some of the related work. Cost function formulation and details of the proposed algorithm are discussed in Section 3. Experimental results are presented in Section 4 and conclusions are made in Section 5.

2. Background and related work

In this section, we first present the general architecture of a memory device with emphasis on phase change memory and then describe related work that discussed PCM lifetime enhancement using write reduction optimization.

2.1. Phase change memory technology

A typical memory device comprises of an array of memory cells as shown in Fig. 1(a). In such array, memory cells are organized into rows and columns, where all of the cells in a row are connected to a common word line and all cells in a column are connected to a common bit line. When accessing data in the array, a row decoder activates all cells in the addressed row (or page). Cell information of all these cells are then transmitted on the various bit lines to the peripheral circuitry which in turn is detected by sense amplifiers and latched in a row buffer. Then, a column decoder selects a subset of the data in the row buffers and connect them to I/O pads.

Phase Change Memory (PCM) is an emerging non-volatile memory technology that stores data by varying electrical resistance of the chalcogenide material in the core memory cell [13,14]. Figure 1(b) shows the structure of a conventional PCM cell which consists of top/bottom electrodes, phase change material, and a heater [13]. Phase change material can switch back and forth between two states: amorphous state that has high resistance and crystalline state that has low resistance. PCM utilizes different resistance levels to store bit information as mentioned earlier. Fig. 2 shows the read and write characteristics of a typical PCM cell [13,14]. To read the state of phase change material, hence cell content, a low current pulse is applied to the memory cell. The bit information is distinguished according to the amount of current transmitted through the cell. To Reset a cell (writing a “0”), a short but high current pulse is applied that will heat the GST material to a temperature above its melting point (620 °C). The current is then removed abruptly hence quenching the GST into the amorphous state. To Set a PCM cell (writing a “1”), a moderate current pulse is applied that would heat the cell's chalcogenide material between crystallization and melting temperature (300 °C - 600 °C). The relatively longer duration of the pulse allows the GST material to crystalize. Thus, a Reset operation takes short time but consumes high current when compared to the Set operation, which requires less current but a longer duration.

Due to varying programming characteristics for Set and Reset operations, previous work have shown that the Reset operation has detrimental effect on cell endurance [27,28]. The extreme heat generated during the Reset operation causes reduced cell lifetime and gives rise to asymmetrical behavior for writing a logic “0” or “1”. Consequently, a good solution to alleviate the endurance problem should favor writing “1”s instead of “0”s. However, most of the reported techniques [19–26] do not take into account such effect. Moreover, a critical reliability issue in PCM is the write disturb problem, also known as thermal crosstalk, which arises from inter-cell thermal distribution. When programming a PCM cell, particularly resetting a cell, the generated heat may disseminate to neighboring cells thus disturbing stored values in idle cells that are in the reset state [29–32]. Write disturbance is a type of soft

Please cite this article as: I. Ahmad et al., Odd/Even Invert coding for phase change memory with thermal crosstalk, Microprocessors and Microsystems (2016), http://dx.doi.org/10.1016/j.micpro.2016.11.015

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