Odd/Even Invert coding for phase change memory with thermal crosstalk

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Cloud based services demand a colossal amount of memory in order to satisfy their objectives. Phase-change memory (PCM) has emerged as one of the most promising memory technologies to feature in next generation memory systems. One of the key challenges of PCM is the limited number of writes that can be performed on memory cells also known as “write endurance”. In this paper we present a cost model which captures the asymmetry as well as disturb characteristics associated with write operations in PCs. Moreover, we present an encoding architecture based on the proposed cost metric to allow the write operation to be performed using minimum cost. The proposed approach called “Odd/Even Invert” re-codes data based on selective inversion of even and/or odd bits to find minimum cost write operation that shall enhance cells lifetime. The proposed approach inquires a cost of only two extra bits regardless of the size of data word used, hence provides a cost effective approach to the problem. Experimental results and comparison with existing techniques on random data, real data, and memory traces from PERSEC benchmark suite, show the effectiveness and scalability of the proposed scheme.

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1. Introduction

Memory has been the key component of computer systems right from the beginning. The convergence of consumer, communication, and data processing applications combined with the rapid growth of cloud computing services have led to an explosive growth in memory requirement [1,2]. At present, DRAM and NAND flash memories together make up 89% of the memory market [1]. The success of DRAM and flash has been essentially attributed to their small cell size and scalability. To meet the ever-growing demand for modern multi-core systems to process data at higher rates, there exist serious challenges that shall limit the dominance of DRAM and flash memories. The unavailability of cost effective scalable lithography for sub-20 nm feature size is one of the factors affecting further evolution of such memories [3]. These challenges have spurred great interest in alternative technologies to shape the landscape of future memory systems. Among the competing contenders, phase-change memory (PCM) has emerged as one of the most promising memory technologies for the next generation memory systems due to its salient features of high density, superior scalability, very low leakage power, low latency, good endurance, long retention (over 10 years), large capacity, byte addressability, shock-resistivity and better reliability compared to other non-volatile memories [4–7].

PCM has better write endurance than flash memory, thus complicated wear-leveling circuitry commonly needed in flash-based systems is eliminated. Further, unlike flash memories where an erase operation is performed on a block, PCM write operations can be programmed at bit level with faster speed without the need for block erase. In addition, PCM requires a lower mask overhead than flash, thereby reducing manufacturing costs for embedded applications. Moreover, PCM integrates well with traditional CMOS processes allowing easy migration to new technologies. Lastly, PCM technology potentially surpasses the scalability of DRAM as well as NAND flash memories [8–11]. Given these advantages, PCM is poised to deliver low cost, easy to manage, high-speed unified memory to usher in the next generation of non-volatile memory solutions [4–12].

PCM is a resistive non-volatile memory that use phase changing properties of chalcogenide alloy (Germanium-Antimony-Tellurium: Ge2Sb2Te5), commonly called GST, to store information by reversibly switching between two states with completely different resistances: high resistance amorphous state that stores value “0”, and low resistance crystalline state that stores value “1” [13,14]. Writing a “0” is commonly referred to as a Reset operation in PCM terminology whereas writing logic “1” is known as a Set. To Reset a cell, a large current is injected into the cell resulting in high temperature that melts the GST material. Then, the current is abruptly...
removed hence quenching the GST into amorphous state. For the Set operation, the current pulse is smaller in magnitude but longer in duration. Therefore, the GST is heated to a temperature between melting and crystallization thus allowing the chalcogenide material to crystallize.

Despite all the advantages of PCM, it exhibits several challenges associated with the write operation such as limited endurance, high energy, and long latency [12,14,15,16]. With respect to cell lifetime and endurance, a typical maximum number of write operations to a PCM cell is limited to $10^9$ write cycles. Even though better than flash, such write endurance characteristic is not sufficient when compared to DRAM memory which has infinite lifetime. In addition, PCM shows asymmetry with respect to the Set and Reset operations [15–18] where Reset consumes higher power than Set, while Set takes longer time. This asymmetrical behavior is ignored by many write schemes such as [19–26], since such approaches assume that writing a bit consumes the same power regardless of the value being written, thus limiting bit write parallelism. Moreover, in such schemes, writing a bit is considered to take an equal amount of time regardless of the value to be written, which is not true, hence can increase write command latency.

The limited write endurance of PCM hinders its widespread usage in computers and embedded systems [12]. Therefore, enhancing PCM lifetime is of great importance especially if is to replace DRAMs in the future. The endurance problem in PCM can be addressed by reducing the number of bits written while serving write requests. Such practice would decelerate the wear out rate and will increase cell lifetime. Consequently, several techniques have been proposed to reduce the number of written bits when servicing writes [16,19–26]. Most of the reported bit-write reduction techniques do not take into consideration write asymmetry and treat bit values of zeros and ones equally. As it was mentioned earlier, writing a “0” takes more current and generate heat above melting temperature which will wear out the cell quickly. Therefore, writing a “0” is more detrimental to cell endurance than writing a “1” [22,23]. Moreover, writing a “0” may give rise to write disturb problem in PCM due to inter-cell thermal crosstalk during programming [29–32]. Write disturbs alter the content of memory cells while operating on others, thus resulting in errors in stored data. Therefore, focusing only on reducing the number of bit flips in write operations does not capture all dimensions affecting the endurance and bit error rate in PCM.

Although the asymmetry of the Reset and Set operation have been considered by some authors for various PCM optimization [17,18,33,34], the authors in [35] has recently introduced CAFO, a simple and an elegant cost model that captures such asymmetry. Based on their cost model, the authors proposed an encoding scheme that is capable of reducing overall cost of write operations. Even though, the decoding process is simple, CAFO’s encoding process is complex and incur a computational overhead on cells write path. Moreover, most of the reported techniques, including those that consider the asymmetry of the write operation such as CAFO [35], do not take into consideration the thermal crosstalk or write disturb in their cost models.

In this paper, we propose a write reduction mechanism, called Odd/Even Invert to improve PCM lifetime. We modified the cost model developed in [35] to include more encoding options and incorporated the effect of write disturbs into the proposed model. The encoding/decoding process proposed is very simple but very effective and is based on selective bit inversion (odd, even, full). The proposed encoding scheme is discussed and presented both at algorithmic as well as architectural level, and it can be easily integrated with existing techniques. Simulation results shows the effectiveness and the scalability of the proposed approach when compared to previously proposed ones. According to best of our knowledge, the proposed approach is the first technique address-
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