



Feasibility study of current pulse induced 2-bit/4-state multilevel programming in phase-change memory



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ABSTRACT

In this brief, multilevel data storage for phase-change memory (PCM) has attracted more attention in the memory market to implement high capacity memory system and reduce cost-per-bit. In this work, we present a universal programming method of SET stair-case current pulse in PCM cells, which can exploit the optimum programming scheme to achieve 2-bit/4state resistance-level with equal logarithm interval. SET stair-case waveform can be optimized by TCAD real time simulation to realize multilevel data storage efficiently in an arbitrary phase change material. Experimental results from 1 k-bit PCM test-chip have validated the proposed multilevel programming scheme. This multilevel programming scheme has improved the information storage density, robustness of resistance-level, energy efficient and avoiding process complexity.

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1. Introduction

Just as IBM announced [1], phase-change memory (PCM) is one of a number of alternative memory structures which has been proposed as a replacement for NAND flash. It exhibits two meta-stable states, namely, an amorphous and a (poly)-crystalline phase of low electrical conductivity and high electrical conductivity, respectively [2]. As PCM widely considered being a potential next-generation non-volatile solid-state memory, it features superior write speed compared to flash memory, negligible standby leakage current, fast read accessing, high cell density and remarkable scalability [3]. For the sake of high information storage density, PCM offers a large signal margin between its two meta-stable phases, and the wide dynamic range also open the door for multilevel cells programming [4].

Nowadays, the increasing demand for high cell density and low power consumption are still the major obstacles to the maturity of PCM technology. Most recently, the feasibility of multilevel storage (MLS) for PCM applications have been emerging, among which MLS approaches are attempting to reduce the programming power and

manufacturing cost in individual bit [5–9]. In order to explore the MLS capabilities, researchers had spared no efforts to carry out strategies, such as core-shell hetero-structured phase-change nanowire [10], stacked cell structure [11–13], novel phase-change material [14–16], and advanced programming algorithm [17,18].

In this work, we proposed SET stair-case current pulse to improve data storage density and robustness of MLS PCM. Since the falling edge rate of SET current pulse is corresponding to phase-change material crystallization rate, multilevel resistances can be induced by stair-case current pulse during partial-SET to full-SET operation. We employed TCAD model to design the PCM cell structure and screen out the SET/RESET conditions. To this end, PCM test chip has been prepared to verify this MLS scheme and our research focused on the SET programming algorithm by controlling the current pulse waveform. In particular, we analyzed both single bit and 1 K bit array programming behaviors of the considered PCM test chip to evaluate the optimum SET condition that affect the feasibility of MLS PCM. A flexible write driver [19] has been proposed to provide a novel stair-case pulses, while a reliable and large sensing margin of read circuit has been designed for PCRAM, leading to an effective write operation and a non-destructive read operation.

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2. Experiment setup and discussions

Our experimental investigation is based on 1 k-bit PCM test chip (bit failure rate 0.195%) under SMIC-130 nm standard CMOS process. As depicted in Fig. 1, the PCM cells having a small cylindrical tungsten (W) bottom electrode (BE) on contact (CT) called lance-type architecture. We chose nitrogen doped $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (N-GST) as active material, and the film thickness is around 120 nm. Ar and N_2 gases were simultaneously introduced into PVD chamber during GST sputtering, and the gas flow ratio of Ar and N_2 is 25:1. The phase-change material N-GST with overlying TiN liner connected to tungsten top electrode (TE). In PCM cells, the BE and TE are connected to the adjacent metal layer as bit line and word line, separately.

Fig. 2 shows a circuit schematic of the PCM array consisting of 8-bit line and 128-word line. 1T1R architecture is defined as N-channel MOSFET (NMOS) accessing phase-change memory cell. A PCM cell programming current can be controlled by biasing the NMOS access device at different gate (word-line, WL) voltages and simultaneously varying the drain (bit-line, BL) voltages. With the gate biasing conditions optimizing, a new multiple trajectory and multilevel current-control algorithm can be realized for MLS programming. The inset shows PCM cell sandwiched between BE and TE, and BE connected to drain terminal. Herein, programming the memory cell in 2 or 4 states is achieved by means of suitable electrical waveforms, which controls the temperature distribution of the active GST volume inside the phase-change memory cell.

3. TCAD modeling

It is an efficient and cost-effect procedure before wafer tape-out that we employed TCAD model to design the PCM cell structure and screen out the SET/RESET conditions. Therefore, in this work, a two-dimensional thermo-electrical TCAD model has been employed to evaluate the programming characteristics of PCM cell. In this model, initial RESET state (Level “11”) has been supposed, and the coupling formulas of Ohm’s law, heat transfer equation, and phase-change kinetics were adopted to simulate this electro-thermal transition. The phase-dependent electrical resistivity and thermal conductivity, temperature distribution and electrical field

distribution are all considered in each subdomain of device. Also, the Johnson-Mehl-Avrami-Kolmogorov [20] equations are introduced to describe the transition from amorphous state to crystalline state, which solves the crystalline volume fraction in active area determined by the phase-change kinetic rate. Based on the established numerical model, the temperature contour plot and phase distribution induced by the input electrical pulse can be observed in real time.

Fig. 3 illustrated the 4-level resistance distribution as a function of programming pulse tail, and the simulated axis-symmetrical phase distribution of PCM cell depicted phase transition proceeding by current pulse with different falling edge in the insets (a)–(d). And it is defined that the PCM cell with red dome region was initially RESET with high resistance state (HRS) (Fig. 3(a)). This statistical result performed by Monte Carlo simulation on TCAD is a solid evidence to predict the device electrical characteristics. The shorter 1st pulse width (40 ns in tail (4)) would induce partial-SET state (higher LRS (“00”)), while the too longer (160 ns in tail (5)) 1st pulse width would lead to full-SET state (lowest LRS) but failing to reversible phase change. The SET stair-case pulse with longer tail (3) performed fully-SET in logic state “00” and “01”, while shorter tail (1) would alleviate SET operation. For the sake of energy-efficient and equal interval distribution, tail (2) with $80 + 7 \times 20$ ns is superior to any other SET condition for multilevel programming. The simulation results indicated that the first SET pulse height and falling edge of SET tail are significant to MLS programming.

4. Programming algorithm and discussions

Conventionally, MLS programming starts with a RESET pulse, and then the active phase-change cell is progressively crystallized with a series of increasing current in the partial-SET regime [21]. However, the bottle neck of MLS programming is how to achieve 4-level resistance with equal logarithm interval. In this work, a current pulse generator (Fig. 4(a)) has been introduced into multilevel current control system, and 6 terminals of SET/RESET pulses, consisting of RSTW (RESET pulse width), RSTH (RESET pulse height), SETOW (1st pulse width), SETOH (1st pulse height), SETW (stair-case pulse width) and SETH (stair-case pulse height), are controlled by periphery circuit. For the sake of energy-efficient

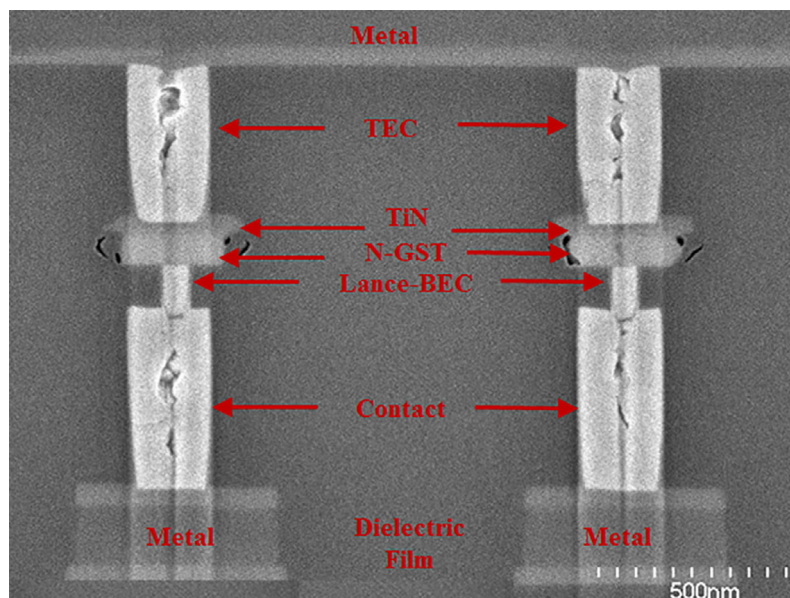


Fig. 1. TEM image of PCM cells, with underlying tungsten lance BEC on the top of contact.

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