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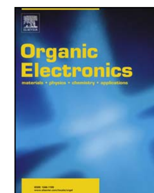

Flexible multi-level resistive memory with high current ratio by electrical triggering into insulating layer

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A B S T R A C T

We demonstrate a flexible multi-level resistive memory device, based on the concept of electrical triggering into an insulating layer, which exhibits a high current ratio between two memory states in the unipolar mode of operation. Due to the presence of a triggering zone in unit memory cell, three resistive memory states having different domain sizes of the conductive filaments are achieved. Each memory state is readable without the disturbances by other states and the current ratio is as high as 10^3. The multi-level memory states are found to be well preserved during bending and applicable for constructing flexible and high-density data storage systems.

1. Introduction

Recently, organic-based resistive memory devices have been paid much attention for non-volatile memories due to their simple structure, large integration density, mechanical flexibility, and solution-processing capability [1–5]. It has been reported that the resistive switching can be achieved through several different mechanisms such as filamentary conduction [6,7], ionic conduction [8], space charge effect [9], and charge transfer effect [10]. Among them, the filamentary conduction is promising for switching device applications from the viewpoint of the scalability as well as the electrical stability [6]. In this case, electrical charges can flow through an insulator between two metal electrodes when conductive pathways along conductive filaments (CFs) are generated by the migration of metal atoms under a localized electric field in the junction area [11]. The CFs are ruptured by either the drift effect of the metal atoms under a negative bias or the thermal fuse effect under a positive bias larger than a threshold for the CF formation [12,13]. According to the rupture process, the switching mode of operation resulting from the filamentary conduction can be classified into a bipolar mode (drift effect) and a unipolar mode (thermal fuse effect) [14,15]. Particularly, the resistive memory in the unipolar mode allows a one diode-one resistance architecture which reduces the crosstalk and simplifies the external circuitry [16,17]. For practical applications, it is important to realize the capability of the multilevel data storage in unipolar switching. More specifically, the growth of the conductive filaments (CFs) should be precisely controlled by the compliance current [18,19] or the magnitude of the voltage [19–22]. For example, the medium resistance state (MRS) with partially grown CFs is indefinitely disturbed during the reading operation so that the reading voltage and the resultant current on-off ratio are not uniquely defined [23,24]. In addition, a series of the voltage pulses are required for regulating the growth of the CFs, which results in the complexity in writing scheme [24,25]. Therefore, it is desirable to achieve well-defined, distinct multi-level memory states, all of which are composed of completely grown CFs.

In this work, we demonstrated an organic multi-level resistive memory device using the concept of electrical triggering into the insulating layer as shown in Fig. 1(a). Our device consists of two electrodes (the top with triggering zones and the bottom being flat) and a polymer insulating layer. Basically, the triggering zone (TZ) of the top electrode formed into the insulator enables to produce the MRS with completely grown CFs, being a stable intermediate state, at a switching voltage in the unipolar mode of operation. As shown in Fig. 1(b), in the presence of two different TZs, four different memory states of a medium resistance state (MRS), a low resistance state (LRS), a very low resistance state (VLRS), and an initial high resistance state (HRS) are available by the application of the corresponding writing voltage (V_{w1}, V_{w2}, and V_{w3}) and the erasing voltage (V_{w0}).

Note that different resistive memory states result from the changes of both the length and the number of the CFs. Since the length of the CFs depends on the separation of two electrodes [26], it is controlled by the depth of the TZ in our case. The application of the first writing voltage (V_{w1}) across the top and bottom electrodes generates the CFs in TZ 1 with a relatively large value of the depth so that the initial HRS is switched to the MRS. Under the second writing voltage (V_{w2}) higher than V_{w1}, the CFs in TZ 1 are partially ruptured by the thermal fuse

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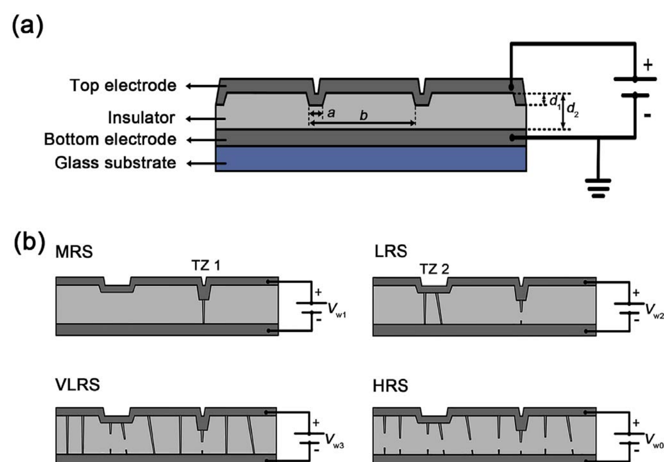

Fig. 1. Schematic diagrams showing (a) the device architecture with the TZs into an insulating layer and (b) the operating principle of our multi-level resistive memory. The width and the depth of the TZ are denoted by a and d_1, respectively. The separation between two adjacent TZs (or period) is b and the gap between the top and bottom electrodes is d_2.

effect [14,15] and the new CFs are grown in TZ 2 with a relatively low value of the depth, yielding the LRS. In the same fashion, the VLRS is obtained at the third writing voltage (V_{w3}). The erasing voltage (V_{w0}) higher than V_{w3} enables to switch the VLRS back to the initial HRS through the rupturing process of all the CFs. Note that the resistive states depend on the width of the TZ in terms of the number of the CFs grown or the area of the unit cell [27]. Note that in principle, it is possible to achieve more than four memory states on the basis of our triggering concept depending on the number of the TZs with different depths and widths in combination with the insulator material. In fact, the multi-level capability depends on the amount of the diffusion of metal atoms into the insulator material, meaning that the number of the TZs should be chosen according to the dielectric property of the insulator.

2. Experimental

Fig. 2(a) shows the fabrication steps of our multi-level resistive memory device with the TZs into an insulating layer. A substrate (glass or polyethylene naphthalate (PEN) for a flexible device) was cleaned under ultra-sonication in acetone, isopropyl alcohol, methanol, and deionized water in sequence for 10 min each. A bottom electrode was made of silver (Ag) of 50 nm thick by thermal deposition over the substrate at the rate of 0.5 Å/s under the pressure of 10^{-6} Torr. For the preparation of an insulating layer, a solution of poly(methyl methacrylate) (PMMA, Sigma-Aldrich Korea) with the molecular weight of 996,000 g/mol in anisole at the concentration of 8 wt% was spin-coated on the Ag electrode at the rate of 3000 rpm for 60 s. The PMMA layer was then soft-baked at 110 °C for 60 min to remove the residual solvent.

For the construction of TZs into the insulating layer of PMMA, predefined patterns of flourinated polymer (Novec™ EGC-1700, 3M) were transfer-printed onto the PMMA layer using an elastomeric stamp made of poly(dimethylsiloxane). Using the fluorinated polymer patterns as etching mask patterns, the insulating layer was then dry-etched using a reactive ion etcher (80 Plus etcher, Oxford Plasma Lab) at 100 sccm of O_2 in 0.1 Torr for 15 s. The geometrical parameters such as the periodicity, the width, and the depth of the TZ shown in Fig. 1(a) were a = 10 μm, b = 110 μm, d_1 = 150 nm, and d_2 = 520 nm. The geometrical profiles of our device were measured using a surface profiler (alpha step 500, KLA-Tencor). The remaining fluorinated polymer was removed under ultra-sonication in a fluoro-solvent (Novec™ 7100, 3M) for 15 min. As the top electrode, a 50 nm-thick Ag layer was then thermally evaporated at the rate of 0.5 Å/s in 10^{-6} Torr. The lateral dimension of our resistive memory device was 1 mm × 1 mm. A part of the microscopic image with the TZs into the insulating layer was shown in Fig. 2(b).

The electrical properties of our multi-level resistive memory device were measured using a semiconductor parameter analyzer (HP4155A, Hewlett-Packard Co.) under ambient environment. In all the electrical measurements, unless otherwise specified, the bottom electrode was grounded and the top electrode was used for the scanning voltage.

3. Behavior of multi-level resistive memory

We first describe the multi-level characteristics of our resistive memory in terms of the writing voltage, the erasing voltage, and the reading voltage together with the current ratio. Note that for all of the resistive memory devices based on the formation of the CFs, the electroforming process, creating percolation paths through the voltage stress, is inevitably required for the initiation of the resistive switching and the stabilization of the resistive memory [28–31]. For example, for an organic resistive memory device with an insulating layer of PMMA, a few tens of the voltage sweeping process was repeated to acquire two stable memory states [32]. In our case, ten times of the sweeping process were performed before the characterization of the multi-level resistive memory.

Fig. 3(a) shows the values of the current (I) as a function of the applied voltage (V) in a step of 0.2 V during three consecutive sweeping processes from 0 to 12 V, from 0 to 26 V, and from 0 to 55 V. The hysteresis in the current during the three sweeping processes was clearly seen from Fig. 3(a). In the first sweep, the current was gradually increased in the initial HRS with the growth of the CFs and abruptly increased at about 11 V according to the formation of fully grown CFs in the TZs, meaning that the MRS was obtained above 11 V. In the second sweep, the current was much larger than that in the first sweep in the same voltage range since the MRS, produced in the first sweep, was preserved. Between 16 V and 20 V, the fully grown CFs in the TZs were partially ruptured and thus the MRS was switched back to the HRS as in the first sweep. On further increasing the applied voltage, the abrupt increase of the current was observed at about 20 V. In other words, the

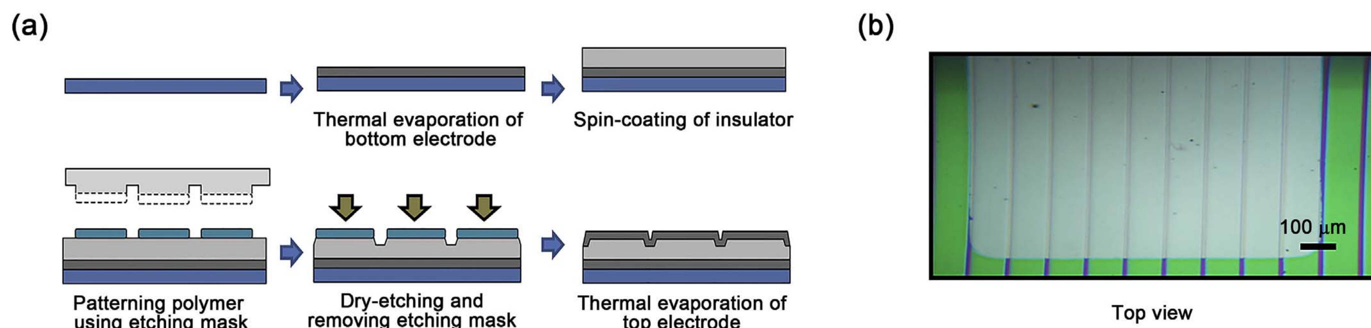

Fig. 2. (a) Fabrication steps of our resistive memory device with the TZs. (b) A part of the microscopic image of our device with the TZs into the insulating layer.

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