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A Pseudo Open Loop Synchronization technique for heavily distorted grid voltage

Ahmed Safa [a,b,*], EL Madjid Berkouk [a], Youcef Messlem [b], Zakaria Chedjara [c], Abdelmadjid Gouichiche [b]

[a] LCP Laboratory, Ecole Nationale Polytechnique, 16200 El-Harrach Algiers, Algeria
[b] Laboratoire de génie électrique et des Plasmas LGEP, Université Ibn Khaldoun, Tiaret, Algeria
[c] Laboratoire ICEPS Université Djilali Liabes sidi Bel ABBES, Algeria

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ABSTRACT

Grid-tied inverters are widely used in the modern power network. The span of their applications varies from power quality enhancement, uninterruptible power supply, grid interface to distributed energy sources, etc. A major aspect of controlling the grid-tied power converter is the synchronization with the main grid. A robust synchronization method is required to maintain the power injection during grid fault and highly distorted grid voltage. This paper introduces a novel Pseudo-Open Loop Synchronization Technique (POLS) based on a fixed reference frame estimator: the Fundamental Positive Components Estimator (PFCE). The algorithm will generate three unitary sinus waveform synchronized with the fundamental positive component of a three-phase grid voltage. Open Loop Synchronization (OLS) technique differs from the closed loop PLL in that it has a faster dynamics response. Two problems may face the OLS: a low-quality main voltage and frequency drift. To face the voltage quality problem, the PFCE is used. This choice is advantageous over the use of a low-pass filter due to the absence of the time delay and filtering performances. For the frequency drift, an optional simple frequency estimator is used. No trigonometric computation is required for the proposed algorithm, making it easy to implement on a low-cost microcontroller. The performances and effectiveness of the proposed method are demonstrated through simulation and experimental results.

1. Introduction

Power converters are widely used in the modern power grid. Their role varies from injecting the active power of distributed energy source, correcting the power factor, power quality enhancement or an uninterruptible power source. In each case, these controllers need to be synchronized with the grid [1]. Hence, the control algorithm of a power converter needs at least one information about the phase angle of the grid voltage at each moment.

The use of static converters enhanced the efficiency and the flexibility of modern electrical machine. Nevertheless, if not well controlled, they could deteriorate the power quality of the main grid. Synchronization with the main grid plays a major role in controlling a static converter. Phase angle detection faces the challenge of accurate detection, response time, and robustness. With the spread of the Distributed Energy Sources (DES) that connects renewable sources to the grid, fast and accurate phase detection are crucial to allow a proper functioning of the DES algorithms. Indeed, meeting the grid codes require more constraints especially in special cases such as Low Voltage Ride Through LVRT requirements [2,3]. Simple methods based on zero crossing [4] is no longer viable. Methods based on signal filtering are prone to slow transients, inaccuracy, filtering delay, etc. [4,5]. Complex methods such as the ones based on Fourier transformer [6], least square estimation [7,8] may have a better accuracy. Nevertheless, due to their complex computation, using them on a modern low-cost microcontroller is very challenging or even impossible.

Phase Locked Loop (PLL) technique is widely used as a signal tracker. A PLL is a linearized control system that synchronizes its outputs with its input's frequency and phase [9]. In power system applications, Synchronous Reference Frame PLL SRF-PLL [10] is a well-known and adopted technique. Nevertheless, performances of the SRF-PLL deteriorate in the presence of unbalance and harmonic contamination. This problem can be mitigated by reducing the bandwidth of the PLLs. However, this technique is not an

* Corresponding author at: Laboratoire de génie électrique et des Plasmas LGEP, Université Ibn Khaldoun, Tiaret, Algeria.
E-mail address: ahmed.safa@univ-tiaret.dz (A. Safa).

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Nomenclature

DES	Distributed Energy Sources
DSOGI	Double Second Order Generalized Integrator
EPLL	Enhanced PLL
FLL	Frequency Locked Loop
HDN	Harmonic Decoupled Network
LF	Loop Filter
LPF	Low Pass Filter
LVRT	Low Voltage Ride Through
MAF	Moving Average filter
MSOGI	Multiple Double Second Order Generalized Integrator
OLS	Open Loop Synchronization
PFCE	Positive Fundamental Component Estimator
PID	Proportional Integral Derivative
PLL	Phase Locked Loop
POLS	Pseudo Open-Loop Synchronization
SRF-PLL	Synchronous Reference Frame PLL
UFPSV	Unitary Fundamental Positive Sequence Voltage
αβCDSC	αβ-frame cascaded delayed signal cancellation
v_{dq}^{p}, v_{dq}^{n}	Positive and negative *dq* voltages
$\hat{v}_{\alpha\beta}$	Estimated Fundamental voltage (Clark components)
$\hat{\omega}$	Estimated grid pulsation
K_f	Loop filter
τ	Loop filter time constant
ω_n, ζ	Natural pulsation and damping factor of H_c
J	Rotation matrix
$H_c(s)$	SRF-PLL closed loop transfer function
$\hat{\Theta}(s)$	Estimated phase angle
$\Theta(s)$	The phase angle
v_d,v_q	Grid direct and quadrature component (Park component)
V_m	Voltage magnitude
V_{uabc}	The three phase unitary voltage
v_{uabc}	Unitary Fundamental Positive Sequence Voltage
$v_{u\alpha}$, $v_{u\beta}$	Unitary Clark components
λ	a damping factor
ω_0	Grid pulsation (314 rd/s)
θ	phase angle of the voltage waveform
θ_0	Initial phase angle of the voltage waveform
K_p	Proportional gain
x_α, x_β	Inputs of the PFCE
$\hat{x}_\alpha$, $\hat{x}_\beta$	Outputs of the PFCE (Estimated fundamental αβ components)
$\hat{x}_{u\beta}$, $\hat{x}_{u\beta}$	Normalized estimated fundamental αβ components

acceptable solution in some application, such as grid-connected distribution generation systems [11] and LVRT requirements [2]. To overcome this limitation, an additional LPF is used in the control loop. Still, this technique suffers from three critical limitations [12]: (1) only an approximation but not the real amplitude and phase angle of the positive sequence component are detected; (2) the detected positive sequence voltages are distorted and unbalanced; (3) the dynamic response of the system is significantly reduced. To improve the performance of the SRF-PLL several synchronization techniques have been reported in the literature. A three-phase Enhanced PLL (EPLL) based on four signal phase and symmetrical components presented in Ref. [13]. The EPLL is accurate under unbalanced grid voltage and has the ability to reduce but not eliminate the effect of harmonic distortion.

Some interesting techniques designed in the double reference frame use a decoupling network to cancel out dynamically the double frequency oscillation created by the voltage unbalance [14,15]. These PLLs achieve a fast and accurate synchronization under unbalanced source voltage. Unfortunately, they are sensitive to the voltage harmonic distortion. MAF-PLL [16] has a simplified structure and provide the robustness under unbalanced and distorted source voltage, but unfortunately, the MAF cause some small inaccuracies when the grid frequency deviates. In addition, the main disadvantage of the MAF is the slow dynamic performance.

Another problem is the design of the control parameters; the conventional approach neglects the dynamics of the filtering stage [11]. However, this approach is not precise. In Ref. [17], an oriented study of the advanced PLLs considering the dynamic of the filtering stage is presented. From the discussion presented in Ref. [17], the advanced PLLs cannot achieve settling time lesser than two cycles due to the aforementioned constraint on the PLL bandwidth. A PID type loop filter can be used to compensate the phase delay caused by the pre-filtering stage. The PLL with the PID LF achieves lesser settling time (1.75 cycles) with high stability compared with PI LF [18]. Other approaches increase the type of the PLL by one (type 3) to improve the dynamic performance of the SRF-PLL. Unfortunately, these approaches worsen the stability problem [7].

Recently, another approach has emerged, the Frequency Locked Loop (FLL) [19–23]. The FLL estimates the frequency of the input signal. Since the frequency is not affected by sudden changes in the main voltage, the performances of the FLL in harmonic rejection and phase angle transient are better than the PLL-based algorithms. A Dual Second Order Generalized Integrator DSOGI-FLL was proposed in Ref. [23]. The DSOGI-FLL had a good performance in the estimation of the fundamental component of the main voltage. However, performances decrease in the case of a heavily distorted voltage [19]. To overcome the drawback of the DSOGI-FLL, MSOGI-FLL is proposed in Ref. [19]. The MSOGI-FLL used multiple DSOGI for each harmonic component and a Harmonic Decoupled Network HDN to eliminate the effect of harmonics. Despite the good performance of the MSOGI-FLL, it has a very hefty computational load (26 μs [19]). A Comb filter is used in Ref. [20] as a pre-filtering stage for a SOGI-FLL to enhance the harmonic rejection. A pre-filtering and filtering stage for the FLL is proposed in Ref. [21]. The latter combines good dynamic response and accurate phase and frequency detection at the expense of the computation time.

Another approach is the Open Loop Synchronization techniques (OLS). These techniques offer a fast dynamic response and unconditional stability [24]. Lately, there has been more interest in developing Open Loop Synchronization (OLS) techniques. To extract the phase angle of the tracked signal, OLS rely on some filtering approaches such as discrete Fourier transformer [25], low pass notch filter [2], Kalman filter [26], αβ-frame cascaded delayed signal cancellation (αβCDSC) operator [24], moving average filter (MAF) [27]. Avoiding the feedback loop came at the expense of accuracy. Since these filters based techniques are sensitive to the signal frequency, a continues information about the frequency must be provided. As a solution, a feedback loop of the frequency is used in Ref. [28].

In this paper, a novel synchronization technique is proposed and named a Pseudo-Open-Loop Synchronization POLS. The term “pseudo” is used to refer to the fact that this method is not “truly” open loop as described in Ref. [24] since it uses the output of the Positive Fundamental Component Estimator (PFCE) to estimate the frequency. However, no regulation is needed in this method, hence, the open loop term. The frequency feedback is optional and can be removed if the frequency of the grid is stable. A significant simplification is introduced by avoiding trigonometric calculation. The presented POLS aims to track and generate a synchronization signal of the main voltage under severe conditions. The flexibility, robustness, and accuracy of the presented POLS allow it to work under any grid voltage condition including an LVRT situation. The simplicity