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Recent results of the ATLAS upgrade planar pixel sensors R&D project

Philipp Weigell*

Max-Planck-Institut für Physik, Föhringer Ring 6, D-80805 München, Germany

ATLAS Planar Pixel Sensors R&D Project

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ABSTRACT

To extend the physics reach of the LHC experiments, several upgrades to the accelerator complex are planned, culminating in the HL-LHC, which eventually leads to an increase of the peak luminosity by a factor of five to ten compared to the LHC design value.

To cope with the higher occupancy and radiation damage also the LHC experiments will be upgraded. The ATLAS Planar Pixel Sensor R&D Project is an international collaboration of 17 institutions and more than 80 scientists, exploring the feasibility of employing planar pixel sensors for this scenario.

Depending on the radius, different pixel concepts are investigated using laboratory and beam test measurements. At small radii the extreme radiation environment and strong space constraints are addressed with very thin pixel sensors active thickness in the range of (75–150) μm, and the development of slim as well as active edges. At larger radii the main challenge is the cost reduction to allow for instrumenting the large area of (7–10) m^2. To reach this goal the pixel productions are being transferred to 6 in production lines and more cost-efficient and industrialised interconnection techniques are investigated. Additionally, the n-in-p technology is employed, which requires less production steps since it relies on a single-sided process.

An overview of the recent accomplishments obtained within the ATLAS Planar Pixel Sensor R&D Project is given. The performance in terms of charge collection and tracking efficiency, obtained with radioactive sources in the laboratory and at beam tests, is presented for devices built from sensors of different vendors connected to either the present ATLAS read-out chip FE-I3 or the new Insertable B-Layer read-out chip FE-I4. The devices, with a thickness varying between 75 μm and 300 μm, were irradiated to several fluences up to 2×10^{16} n_{eq}/cm^2. Finally, the different approaches followed inside the collaboration to achieve slim or active edges for planar pixel sensors are presented.

1. Upgrades roadmap

Presently, the ATLAS pixel detector [1] comprises three barrel layers located at radii between 50.5 mm and 122.5 mm as well as three end-cap discs on each side of the detector. In total about 80 million read-out channels are distributed on 1744 pixel modules. Each module is composed of a 250 μm thick n-in-n planar silicon sensor interconnected via the solder bump bonding technique [2] to 16 FE-I3 read-out chips [3], featuring pixel pitches of 50 μm × 400 μm. Sensors and read-out chips are specified up to a fluence of 10^{15} n_{eq}/cm^2 (1 MeV neutrons) or a dose of 500 kGy.

To increase the physics reach of the LHC programme, it is foreseen to upgrade the accelerator chain in three dedicated long shutdowns (LS), followed by longer data-taking phases, called phase 0, I, and II. While increasing the beam energy to its design value, the peak luminosity will increase eventually up to $(5–8) \times 10^{34}$ cm^{-2} s^{-1} [4]. Each LS will be mirrored by upgrades to the ATLAS detector to cope with the increased luminosity. This paper will focus on the upgrades of the pixel detector, only. The first LS starts beginning of 2013 and lasts until the end of 2014; it will lead to an approximately fourfold increase in luminosity. In the ATLAS detector a new fourth pixel layer will be mounted on a new smaller beam pipe at a radius of 32 mm. This is referred to as the Insertable B-Layer (IBL) [5]. The smaller radius inhibits overlapping modules in z as employed in the present ATLAS pixel detector. Thus, the active fraction had to be increased, using a new design of the n-in-n sensors discussed in Section 3.2.1. Given the harsher radiation environment and the higher occupancy a new read-out chip, the FE-I4 [6], was developed, which is specified up to a received fluence of 5×10^{15} n_{eq}/cm^2. The pixel cell size was reduced to 50 μm × 250 μm and the number of pixel cells increased from 2880 to 26,880. While the upgraded pixel detector is believed to retain sufficient tracking capabilities after the second LS, which starts around 2017, during the third LS from 2021 to 2022 a major upgrade of the entire inner tracking system is planned. The replacement of the

* Tel.: +49 8932354416.
E-mail address: Philipp.Weigell@mpp.mpg.de

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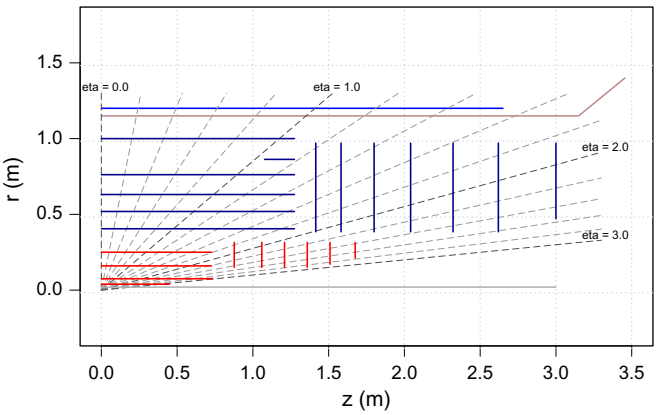

Fig. 1. Baseline layout of the new inner detector for the Phase II upgrade [7]. Pixel (strip) layers and discs are indicated in red (blue). (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

tracking detector is required given the foreseen fluences in phase II of up to 2×10^{16} n_{eq}/cm^2 in the innermost layer, along with the very high occupancies, calling for higher granularity and a new generation of read-out chips for the inner layers. The current baseline layout planned is depicted in Fig. 1. The barrel consists of four pixel layers, with a minimal radius around 39 mm and a maximal radius around 250 mm. Six pixel discs are foreseen for the forward region, i.e. at a pseudorapidity of about $1.8 \leq |\eta| \leq 2.8$. Depending on performance simulations, it is planned to increase the radius even further, or to add an additional fifth pixel layer.

2. The ATLAS planar pixel sensor R&D project

The scope of the ATLAS Planar Pixel Sensor R&D Project is to evaluate and improve the performance of planar pixel sensors for these detector upgrades as well as to determine their operation conditions in this high luminosity environment. Planar pixel sensors are used widely already in present high energy physics experiments and have very well established manufacturing processes with very high yield and low costs. Still, at the irradiation levels expected in the inner pixel layers at the HL-LHC, they require high bias voltages and pose stronger constraints on the cooling systems, especially when comparing to emerging sensor technologies like 3D sensors [8], which still are affected by lower yield and higher production costs, but made significant progress over the last few years and will be used in the ATLAS IBL upgrade [9–11]. Besides radiation hardness studies, geometry optimization and cost reduction are the key topics, which will also be covered in this paper. To achieve these goals, sensor productions from CiS [12], FBK [13], HPK [14], Micron [15], MPI-HLL [16], and VTT [17] are used. To investigate the properties for realistic scenarios, irradiations with various particle types and energies are used, i.e. reactor neutrons (JSI) [19], and protons with 26 MeV (KIT) [18], 800 MeV (LANSCE) [20], and 24 GeV (CERN PS) [21]. The samples are then measured in the laboratory using radioactive sources and in beam test at the CERN SPS and DESY, where the EUDET beam telescope [22] is employed. The experimental measurements are supported by TCAD simulations.

3. Phase II requirements

Investigations within the ATLAS Planar Pixel Sensor R&D Project are focusing towards the phase II upgrade of the ATLAS inner tracking system. The results presented in the following are grouped according to the radius they are most relevant for.

3.1. Phase II – outer layer

The outer pixel layers drive the total area to unprecedented values of about (7–10) m^2, thus cost effective modules are mandatory. To achieve this, cost-reduction for the sensors as well as for the interconnection is envisaged. Since the latter one is mostly driven by the number of tiles to be interconnected, it is foreseen to use large area sensors, which are then interconnected to four or even six FE-I4 chips. Three productions are ongoing at the moment which include either four chip sensors or have pairs of two-chip sensors placed close on the wafer, such that they can be diced as a four-chip sensor. The sensors were designed by the KEK group [23], the University of Liverpool group, and the MPP/HLL group, and are produced by HPK, Micron, and CiS respectively.

3.1.1. Performance of n-in-p pixel detectors

Since the pn-junction is on the pixel implantation side in n-in-p sensors, the guard rings can be placed on the front-side as well, and thus patterned processing is only needed on a single side. Consequently, no masks and no alignment for back-side processing are needed, lowering the cost and enabling the use of more foundries for processing. Furthermore, the lack of patterned back-side implantations eases subsequent handling and testing. A possible problem connected to the n-in-p geometry is related to the high voltage present at the edges at the front-side, transferred from the backside through crystal damages along the sensor sides. Since the sensor edge region is facing the read-out chip, which is at ground potential, at a distance of O(10 μm), destructive electric discharges are possible and were observed [24]. To prevent this, three different methods were investigated. In the first approach a 3 μm benzocyclobutene (BCB) [25,26] passivation layer on the sensor surface was used and no destructive discharge observed up to a bias voltage of 1 kV [27]. As alternatives two post processing approaches, employing silicon adhesive and Parylene-C have been investigated. Up to 1 kV no destructive discharges were found when using a full silicon adhesive encapsulation of the module. Modules encapsulated with Parylene-C have been tested up to 650 V, and again no destructive discharges were seen. In none of the three approaches a degradation of the high voltage insulation was observed after irradiation.

An extensive radiation programme, using sensors from three different productions, was conducted to investigate the performance of n-in-p pixel modules after high received fluences up to 10^{16} n_{eq}/cm^2. The first production using designs by the MPP/HLL group was processed at CiS on 285 μm thick wafers [27]. The other two productions yielded 150 μm thick sensors and were conducted by the KEK group in collaboration with HPK [28,29] and by the MPP/HLL group [30,32].

In Fig. 2 the most probable values (MPVs) of the collected charges are summarised as a function of the applied bias voltage for various received fluences for the modules from the CiS production. The MPV of the collected charge rises with bias voltage and decreases with received fluence. For all modules the collected charge exceeds the threshold of 3.2 ke by a factor of 2 with bias voltages below 1 kV, indicating a good hit efficiency. For comparison measurements using an n-in-n irradiated module [35] are shown as well.

With beam test measurements at the CERN SPS employing 120 GeV pions and at DESY using 4 GeV positrons the hit efficiency was determined as a function of the bias voltage and received fluence for several modules from the different productions. For a module from the CiS production, irradiated to a fluence of 10^{16} n_{eq}/cm^2, and operated at a moderate bias voltage of 600 V for a threshold tuned to 2 ke the mean hit efficiency was determined to be still as high as $(97.2 \pm 0.3)\%$. In Fig. 3 the hit