# Design Techniques for Load-Independent Direct Bulk-Coupled Low Power QVCO

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***Abstract*—Design techniques for a load-independent low-power low-phase-noise CMOS *LC* direct bulk-coupled quadrature voltage-controlled oscillator (DBC-QVCO) is presented in this paper. A capacitor tapping technique is used to lower the phase noise and achieve load-independent frequency of oscillation. Class-C operation is used to further reduce the phase noise and power consumption. Quadrature coupling is achieved using bulk coupling, leading to reduction in both power and area. The DBC-QVCO has been implemented in a standard 0.18-$\mu$m BiCMOS process and occupies an area of 0.3 mm$^2$. The implemented DBC-QVCO achieves a measured phase noise of −114.2 dBc/Hz at 1-MHz offset from the 6.26-GHz carrier while consuming only 3.2 mW from a 1-V power supply. The DBC-QVCO achieves a figure of merit (FOM) of −185.1 dBc/Hz and an FOM with area of −190.3 dBc/Hz, which are among the best compared with recently published QVCOs operating in a similar frequency range.**

***Index Terms*—Bulk-coupling, class C, flicker noise, load-independent VCO, quadrature voltage-controlled oscillator (QVCO).**

## I. Introduction

QUADRATURE signals play an important role in many modern transceivers. In order to attain desirable performance, quadrature signals with very low phase noise should be able to be generated while consuming very low power. Also, in order to attain better power optimization, quadrature signal generation needs to achieve load-independent frequency of oscillation. Currently, there are four major ways to generate quadrature signals. Frequency dividers [1] are widely used, but they inherently consume more power as the VCO needs to be operated at twice the desired frequency. Another way is to use polyphase filters [2]. However, these filters have higher loss and, hence, require buffers for signal amplification and thus end up consuming higher power. Ring oscillators are most convenient for multiphase generation, but they inherently suffer from poor phase-noise performance [3]. The fourth way would be to use quadrature voltage-controlled oscillators (QVCO)s, which can generate quadrature signals with superior phase noise at low power consumption. Therefore, QVCOs have proved to be critical components in applications that require high-fidelity quadrature signals such as in wireless and wireline transceivers.

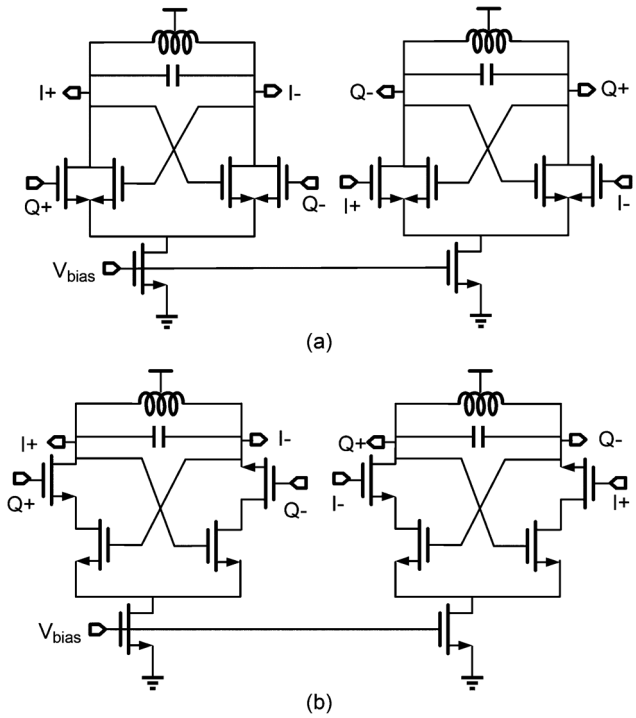


Fig. 1. Schematic of traditional QVCOs. (a) P-QVCO. (b) S-QVCO.

The most attractive and popular approach to implement a QVCO is to couple two symmetric *LC*-tank VCOs to each other to take advantage of the low phase noise of *LC* VCOs [4]–[6]. Traditional *LC* QVCOs can be classified as parallel-coupled QVCO (P-QVCO) and series-coupled QVCO (S-QVCO), as shown in Fig. 1(a) and 1(b), respectively. For P-QVCOs, the coupling transistors are placed in parallel with the switching pairs, which causes a nonzero resonator phase shift and thus degrades the phase noise of the QVCO [7]. The S-QVCO reduces voltage headroom and requires more power consumption due to

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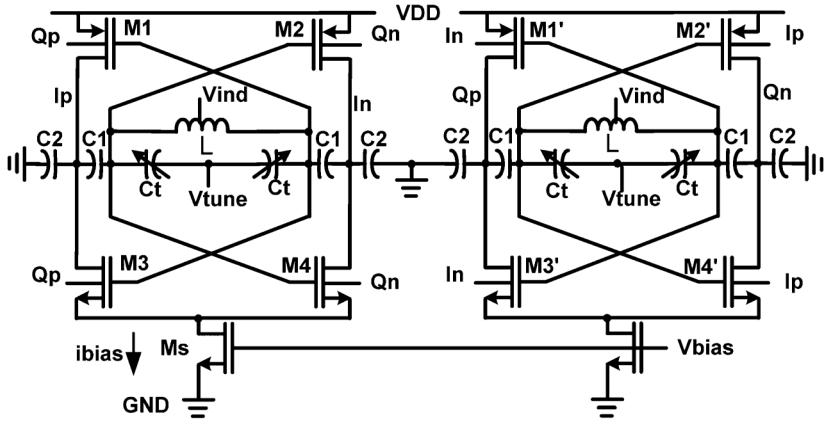


| Component | Value |
|---|---|
| M1 | 54μ/0.18μ |
| M3 | 24μ/0.18μ |
| C1 | 100 fF |
| C2 | 150 fF |
| L | 1.4 nH |
| Ct (mos_var) | 18μ/0.5μ |
| Ms | 200μ/1μ |
| ibias | 1.6 mA |
| VDD | 1 V |

Fig. 2. Proposed bulk-coupled load independent *LC* QVCO.

the stacked transistors for series coupling [8]. To reduce power consumption while retaining low phase noise, a bulk-coupling technique has been applied in QVCOs [9], [10]. However, all of these techniques are load-dependent and require the use of a buffer, thus consuming higher power. In order to tackle loading effects on frequency of oscillation, a capacitor tapping (CT) technique was proposed in [11], but its effect on phase noise has not been shown.

In this paper, we describe in detail the design techniques for a novel DBC-QVCO topology consisting of two load-independent *LC* VCOs proposed in [12]. Quadrature coupling is achieved by injecting the output of one VCO into the bulks of the cross-coupled nMOS and pMOS pair of another VCO. Lower threshold voltage is achieved by forward bulk biasing, which provides more voltage headroom and allows for complementary VCO topology. The CT technique is also used in the proposed DBC-QVCO to achieve load independence and lower phase noise. Class-C operation of the cross-coupled pair is used to reduce noise and power consumption. The remainder of this paper is organized as follows. In Section II, we present our proposed design. Section III describes chip implementation and measurement results. Finally, we conclude the paper in Section IV.

## II. Proposed Circuit Design

The proposed bulk-coupled complementary *LC* DBC-QVCO architecture is shown in Fig. 2. Because of larger transconductance and waveform symmetry, complementary VCO provides better phase-noise performance and faster start-up as compared with an nMOS- or pMOS-only *LC* VCO [13]. Hence, complementary VCO architecture has been adopted in this design. $M1$, $M2$ and $M3$, $M4$ form a complementary cross-coupled pair. Note that the devices are capacitively cross-coupled. Such a configuration is useful in biasing the gate of switching devices independently and sustain larger swing at the tank. The VCO output $Qn$ is directly coupled to bulks of $M2$ and $M4$, and $Qp$ is coupled to the bulks of $M1$ and $M3$. Outputs $In$ and $Ip$ are also coupled in the same way. Coupling through both nMOS and pMOS has the advantage of achieving a higher coupling factor which is essential to keep low phase error [14]. Inductor $L$ and varactors $Ct$ form the tank core while C1 and C2 are used as tapped capacitors. The design techniques used to attain better performance for the DBC-QVCO are described further.

### A. Direct Bulk Coupling

Coupling in the proposed QVCO is achieved by direct bulk coupling. With this bulk-coupling approach, additional parallel- or series-coupling transistors required in traditional QVCO are eliminated. The common-mode voltage of the output signals forward biases the junction diode of these transistors to achieve lower threshold voltage for low-voltage operation. This reduction in threshold voltage provides larger voltage headroom as required by stacked nMOS and pMOS pairs in a complementary structure. Forward biasing of the bulk also helps to reduce flicker noise in pMOS [15]. Reduction of flicker noise improves phase noise, especially at offset frequency close to the carrier, which is important for the frequency synthesizer to achieve fine frequency resolution [16]. Since bulk coupling leads to a coupling factor of less than unity, better phase noise can be achieved [17].

To study the effect of direct bulk coupling (both dc and ac) on phase noise, we need to estimate its effect on drain–current