Low Thermal Budget Monolithic Integration of Evanescent-Coupled Ge-on-SOI Photodetector on Si CMOS Platform

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***Abstract*—The design and fabrication of a monolithically integrated evanescent-coupled Ge-on-silicon-on-insulator (SOI) photodetector and CMOS circuits were realized on common SOI platform using an "electronic-first and photonic-last" integration approach. High-performance detector with an integrated Si waveguide was demonstrated on epitaxial Ge-absorbing layer selectively grown on an ultrathin SOI substrate. Performance metrics of photodetector designs featuring vertical and lateral PIN configurations were investigated. When operated at a bias of -1.0 V, a vertical PIN detector achieved a lower $I_{\rm dark}$ of $\sim$0.57 μA as compared to a lateral PIN detector, a value that is below the typical $\sim$1 μA upper limit acceptable for high-speed-receiver design. Very high responsivity of $\sim$0.92 A/W was obtained in both detector designs for a wavelength of 1550 nm, which corresponds to a quantum efficiency of $\sim$73%. Impulse response measurements showed that the vertical PIN detector gives rise to a smaller full-width at half-maximum of $\sim$24.4 ps over a lateral PIN detector, which corresponds to a -3 dB bandwidth of $\sim$11.3 GHz. *RC* time delay is shown to be the dominant factor limiting the speed performance. Eye patterns (pseudorandom binary sequence 2^7-1) measurement further confirms the achievement of high-speed and low-noise photodetection at a bit rate of 8.5 Gb/s. Excellent transfer and output characteristics have also been achieved by the integrated CMOS inverter circuits in addition to the well-behaved logic functions. The introduction of an additional thermal budget (800 °C) arising from the Ge epitaxy growth has no observable detrimental impact on the short-channel control of the CMOS inverter circuit. In addition, we describe the issues associated with monolithic integration and discuss the potential of Ge-detector/Si CMOS receiver for future optical communication applications.**

***Index Terms*—CMOS circuit, germanium, integrated photonics, near infrared, photodetector, silicon-on-insulator (SOI).**

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I. Introduction

THE CONVERGENCE of electronic–photonic integrated circuit is becoming increasingly important to keep up with the performance roadmap known as Moore's law [1]. Today, data transmissions at a bit rate of 10 Gb/s over long distance makes photonic interconnection an easier approach to implement than electrical interconnect. At this data rate, the conventional copper solution has begun to encounter extreme challenges related to power consumption and reach [2]. Pushing every gigabits of data through these copper wires has become much more expensive and complicated as it requires sophisticated techniques to overcome the distortion caused by the imperfection in the copper lines. Moreover, the growing issues in electromagnetic interference, signal crosstalk, and heavier weight make it an inferior approach for high-bandwidth applications [3]. To keep up with the scaling of interconnect bandwidth, an alternative solution makes use of optical interconnect technology to address the ever increasing bit rate requirement of data communication. However, the cost and form factor of conventional high-speed optical devices have been the major showstopper to the introduction of this technology for short-reach interconnect applications.

Over the past decades, conventional optical components were typically made of exotic III–V compound materials such as gallium arsenide (GaAs) and indium phosphide (InP) due to their excellent light emission and absorption properties. Unfortunately, compound-semiconductor devices are generally too complicated to process and costly to implement in optical interconnects. In search for a cost-effective solution, Si photonic emerges to hold great promise for its inexpensive material and its compatibility with current CMOS fabrication technology [4]. Recent advancements have also shown that silicon (Si) is a viable optical material suitable for high-bandwidth data communication applications. In addition, the feasibility of converging photonic and electronic integrated circuits (EPICs) all on a single chip makes it an extremely attractive option to extend the performance roadmap as driven by Moore's Law [1], [5].

However, to make silicon photonic communication a reality, several key technological challenges have to be addressed. Inferior optical properties of Si [6] have thus far the major showstopper to preclude the development of a key active photonic component needed for near-infrared optical detections. Very recently, Ge has attracted growing interest for the realization of high-performance photodetector [7]–[17] due to its large absorption coefficient [18] and its pseudodirect bandgap property.

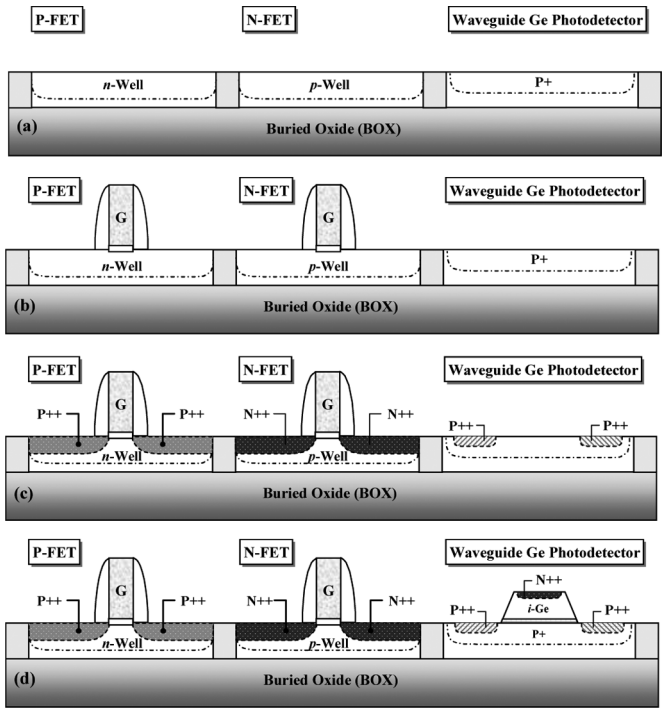

Fig. 1. Schematic showing the "electronic-first and photonic-last" integration approach for monolithically fabricating the evanescent-coupled Ge p-i-n photodetector and Si CMOS circuit on common SOI platform.

However, Ge can be a challenging material to integrate in a CMOS environment for its low thermal budget constraint and its large lattice mismatch of ∼4.2% with Si [19]. High defect densities seen in the Ge-on-silicon-on-insulator (SOI) epitaxial film could induce unfavorable carrier recombination process that would degrade the detector's performance.

In this paper, we describe our design and fabrication strategy toward realizing a monolithically integrated Ge photodetector and CMOS circuits on common SOI platform for high-speed receiver applications. The approach, based on the Ge-on-SOI technology, enables the realization of high-sensitivity and low-noise photodetector that is capable of performing efficient optical-to-electrical encoding in the near-infrared wavelengths regime. We explore photodetector designs with both vertical and lateral PIN configurations and elucidate the merits of these devices in terms of their dark current, responsivity, and bandwidth performance. In addition, we evaluate the dc characteristics of the monolithically fabricated CMOS inverter circuit. We assess the impact of the additional thermal budget arising from the Ge epitaxy growth on the threshold voltage variation of short-channel CMOS transistors and discuss the issues and potential for seamless integration of electronic and photonic integrated circuits.

II. Device Fabrication and Material Characterization

Fig. 1 shows the "electronic-first and photonic-last" integration approach adopted for monolithically fabricating the Ge photodetector and CMOS integrated circuit on common SOI platform. Starting SOI substrate with a thin overlying Si layer thickness of ∼220 nm and a buried oxide thickness of ∼2 μm was used. Channel waveguide with a width of ∼200 nm was first formed by using the same Si mesa isolation process employed for proper electrical isolation. A good control of the sidewall profile was achieved for enabling low waveguide transmission loss. Using a thin sacrificial oxide, selective ion implantations were first performed to define the p-well and n-well regions of the n-MOS and p-MOS transistors, respectively [see Fig. 1(a)]. A moderately high p-type doping was also implanted on the detector's active region, in which the dose was carefully chosen to allow low series resistance while not impacting the quality of the as-grown Ge epitaxy film. Rapid thermal annealing at 1030 °C for 5 s was used to activate the dopant. After removing the sacrificial oxide, a thin gate oxide of ∼50 Å was formed by thermal oxidation and a low-pressure chemical vapor deposition (LPCVD) polysilicon of ∼100 nm was deposited and patterned to form the transistor gate electrodes [see Fig. 1(b)]. A thin sidewall spacer made of conformal oxide was deposited and followed by an anisotropic reactive ion etch. Deep source/drain implants for p++ and n++ regions were subsequently performed for the CMOS transistors and rapid thermal annealing at 1030 °C for 5 s was employed to activate the dopant. Simultaneously, the bottom contact of the Ge photodetector was also formed using a highly doped p++ region [see Fig. 1(c)]. A plasma-enhanced chemical vapor deposition (PECVD) passivation oxide layer of ∼600 Å was then deposited and patterned to open the Ge active window. Selective epitaxial growth of Ge was performed in an ultrahigh vacuum chemical vapor deposition (UHVCVD) epitaxy reactor. The selective Ge epitaxy process commenced with the deposition of a 20-nm silicon–germanium (SiGe) buffer and a 30 nm pure Ge seed layer. This was followed by the low-temperature Ge epitaxy performed at 550 °C [20]. High-quality Ge epitaxial film with a thickness of ∼500 nm was selectively grown on the detector's active region to form the absorbing layer for near-infrared wavelengths detections. A Ge surface roughness of ∼0.35 nm was measured using atomic force microscopy (AFM) and a dislocation defects density on the order of $\sim 10^7$ cm^{-2} was determined using the etch-pit density (EPD) approach. The achievement of such low defects density is predominantly due to the insertion of a thin SiGe buffer layer grown using a low temperature approach. This is so because the low-temperature SiGe buffer plays a role in providing Ge dangling bonds as nucleation sites to ease the selective Ge epitaxy process. Moreover, such SiGe buffer also acts as an additional interface to relieve the large lattice mismatch strain of ∼4.2% between the Ge and the Si substrate [21]. As a result of such low defects level within the Ge film, postepitaxy Ge anneal was skipped to reduce the thermal budget.

High dose selective phosphorous implant was then performed and annealed at 500 °C for 5 min to form good n-type ohmic contact for the Ge detector. Following passivation oxide deposition, contact and metallization were subsequently done to complete the device fabrication. The SEM images of the Si CMOS circuit and the monolithically integrated Ge p-i-n photodetector were shown in Fig. 2(a) and (b), respectively. Transmission electron microscopy (TEM) micrograph of the completed Ge detector is shown in Fig. 3(a). The insertion of a SiGe buffer layer reduces the lattice mismatched between Ge and the Si substrate, which