Phase-Locked Loop Based on Selective Harmonics Elimination for Utility Applications

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Abstract—**Phase-locked loops (PLL) are widely used in power electronics equipment connected to the mains. The use of a square wave voltage-controlled oscillator instead of a sinusoidal one eliminates one multiplier, resulting in a simple PLL algorithm, suitable for low-cost processors. In spite of its simplicity, distorted grid voltages cause steady-state phase error. This paper proposes the use of a modified square waveform obtained by the selective harmonics elimination (SHE) method to solve the phase error problem. Simulation and experimental results for the steady state and the transient tests are presented to validate the proposed single-phase and three-phase SHE-PLL methods. The tests using a field-programmable gate array show that the dynamic response of the proposed method is similar to that of classical PLL, with a simpler implementation.**

Index Terms—**Field-programmable gate arrays (FPGA), phase-locked loops (PLL), power electronics.**

I. INTRODUCTION

PHASE-LOCKED loops (PLLs) are widely used in communication, control, automation, and instrumentation systems to achieve signal synchronization. Recently, PLLs have found many applications in grid-connected power electronic devices: 1) to synchronize thyristor firing circuits [1]; 2) to transform variables between stationary and synchronous rotating reference frames [2], [3]; 3) to compute power system disturbances in power quality monitoring systems [4], [5]; and 4) to calculate reference signals for the internal control loops in uninterruptible power supplies [6], dynamic voltage restorers [2], [5], active filters [5], and power converters used in distributed energy systems [3], [7], including wind and photovoltaic systems [8]. In these applications, the PLL detects the phase angle and frequency of the grid fundamental voltage. On the other hand, three-phase PLLs detect the positive sequence component, even for distorted and unbalanced grids [3], [9]–[20].

The typical PLL [21], [22] is composed of a phase detector (PD), a loop filter (LF), and a voltage-controlled oscillator (VCO) (see Fig. 1).
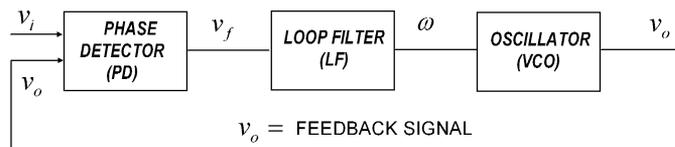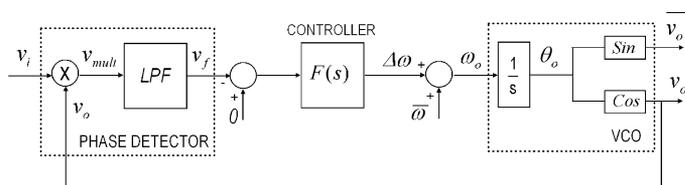
Fig. 1. PLL—general structure.

Fig. 2. Classical single-phase PLL.

The PD compares the reference signal v_i with the feedback signal v_o, producing a signal v_f that depends on the phase error between v_i and v_o. All the cases discussed in this paper use the linearized multiplier type PD [20]–[22] followed by a low-pass filter (LPF). The LF attenuates the oscillating terms of the error signal v_f. The VCO generates an output signal v_o with frequency ω. The complete system produces an output signal v_o, synchronized in phase and frequency with the reference signal v_i.

Often the feedback signal v_o is a unit amplitude sinusoidal signal [1]–[11], [23], [24]. This strategy is defined in this paper as a classical PLL.

In [21] and [22], the sinusoidal VCO was replaced by a square wave VCO for analog implementation. This method does not need an analog multiplier in the PD block and is suitable for hardware implementations with pure sinusoidal input. The product of v_i by a two-level (± 1) signal v_o was accomplished by mixed analog/digital circuitry. Nowadays, the square wave strategy can be useful for PLLs implemented in microcontrollers, DSPs, and field-programmable gate arrays (FPGA). In this paper, the PD in Fig. 2 that computes the product $v_{\text{mult}} = v_o \cdot v_i$ in the classical PLL is replaced by the operation $v_{\text{mult}} = \text{sign}(v_o)$, eliminating one multiplier. Another advantage compared to the classical PLL is to reduce memory usage associated with long lookup tables required to store the sinusoidal waveforms with reasonable accuracy.

According to [22], the square wave PLL is not applicable to input signals with harmonics, because the steady-state phase error is not null. We propose an improvement on the square wave PLL which consists in substituting the original square wave by the selective harmonics elimination (SHE) waveform, thus minimizing the PLL phase angle error.

This paper is organized as follows. Section II reviews the operation of the classical PLL, emphasizing that it synchronizes with the fundamental component of the input signal v_i. Section III describes the square wave PLL. Section IV discusses the operation of the square wave PLL, explaining why the phase error increases with distorted input signals.

The PLL phase error is computed as a function of the spectrum of the grid voltage. Section V discusses the requirements for the pulsewidth modulated squared SHE waveform and the evaluation of its switching angles. Section VI presents simulation and experimental results for both steady state and transient tests of a single-phase PLL, validating the proposed SHE-PLL method. The tests were carried out using an FPGA. The three-phase SHE-PLL is analyzed in Section VII, where experimental results are shown. The square wave PLL and the SHE-PLL algorithms present a dynamic response similar to the classical PLL. Notwithstanding, they are implemented in a simpler way. Section VIII concludes this paper.

II. CLASSICAL SINGLE-PHASE PLL

Fig. 2 shows the topology of the classical single-phase PLL, using a multiplier type PD.

Let the input voltage be represented by

$$v_i = A_1 \sin\left(\omega_1 t + \phi_1\right) + A_2 \sin\left(2\omega_1 t + \phi_2\right) + \dots$$

$$= \sum_{k=1}^{\infty} A_k \sin\left(k\omega_1 t + \phi_k\right) \tag{1}$$

where A_1 is the fundamental peak value, ω_1 is the fundamental angular velocity (frequency), $\overline{\omega}$ is the grid nominal frequency, and ϕ_1 is the fundamental phase angle. The feedback signal v_o, which is the PLL output with unit amplitude, is a sinusoidal voltage represented by

$$v_o = \cos\left(\omega_o t + \phi_o\right) = \cos\theta_o. \tag{2}$$

The signal v_{mult} is computed in the Appendix by calculating the multiplier output $v_{\text{mult}} = v_o \cdot v_i$ in (A.1) and by considering that v_o tracks v_i, i.e.,($\omega_o = \omega_1$) in (A.2). The signal v_{mult} presents a dc and oscillating components. Keeping in mind that v_i contains odd and even harmonics, the oscillating terms of v_{mult} are thus multiples of the mains fundamental frequency ω_1.

The LPF block is designed to guarantee that the high frequency components of v_{mult} are attenuated; thus, the steady-state filtered output v_f can be described by

$$v_f = \frac{A_1}{2} \cdot \sin\phi_d. \tag{3}$$

In this paper, the LPF block in Fig. 2 is implemented using a moving average filter (MAV) [5], [14], [18]–[20]. The MAV filter with a window length T, corresponding to the fundamental frequency period, eliminates all the oscillating terms of v_{mult} that are multiples of the fundamental frequency ω_1. According to (A.2), if v_i contains only odd harmonics, the oscillating terms of v_{mult} are multiple of $2\omega_1$. In this case, a MAV with a window length of $T/2$ can be used, resulting in lower memory usage and faster LPF response [14].
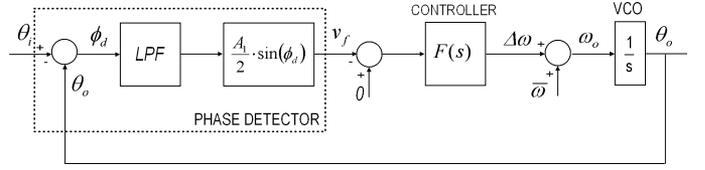

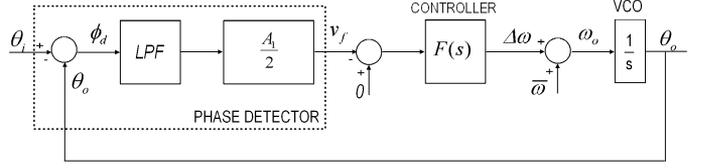Fig. 3.   Nonlinear single-phase PLL dynamic model.
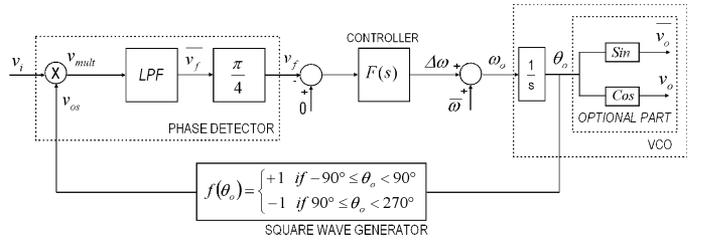

Fig. 4.   Linearized single-phase PLL model.

Fig. 5.   Square wave feedback signal PLL.

Equation (3) leads to the nonlinear model shown in Fig. 3. The phase error is $\phi_d = \theta_i - \theta_o$. Considering $\theta_i = \omega_1 t + \phi_1$ and $\theta_o = \omega_o t + \phi_o$, when $\omega_1 = \omega_o$, the phase error is equal to $\phi_d = \phi_1 - \phi_o$.

If ϕ_d is very small, then $\sin\left(\phi_d\right) \cong \phi_d$ and the linearized model in Fig. 4 is obtained.

Note that the closed-loop gain of this PLL is highly dependent on the peak amplitude of the fundamental voltage A_1, as seen in (3). Normalization of the input voltage has been suggested in [9] to minimize the effects of grid voltage variations on the PLL dynamic response.

For the stable steady-state operation point, $\phi_d = 0$, $v_f = 0$ and v_o are in quadrature with the input voltage v_i. The signal $\overline{v_o}$ in Fig. 2 is in phase with the input voltage v_i.

III. SQUARE WAVE FEEDBACK SIGNAL PLL

The single-phase square wave PLL, shown in Fig. 5, has the same structure of the classical PLL in Fig. 2. However, it uses the square wave v_{os} (see Fig. 6) instead of using the output voltage $v_o = \cos\left(\omega_o t + \phi_o\right) = \cos\theta_o$ as feedback signal to the PD. The signal v_{os} is obtained at the output of the square wave generator and depends on the phase angle θ_o according to the function $f\left(\theta_o\right)$ defined in Fig. 5.

The first component of the Fourier series expansion of v_{os} is proportional to the sinusoidal signal v_o, suggesting that the behavior of the square wave PLL is similar to the classical PLL. The gain $\pi/4$, which is added to keep the closed-loop gain constant for all presented PLLs algorithms, will be derived in Section IV-A. Performance loss due to the harmonic components of v_{os} will be discussed in Section IV-B. One advantage of a