# 1-Bit Sub Threshold Full Adders in 65nm CMOS Technology


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**Abstract: In this paper a new full adder (FA) circuit optimized for ultra low power operation is proposed. The circuit is based on modified XOR gates operated in the subthreshold region to minimize the power consumption. Simulated results using 65nm standarad CMOS models are provided. The simulation results show a 5% - 20% for frequency ranges from 1 KHz to 20MHz and supply voltages lower than 0.3V.**
**Keywords**: Full adder, ultra low power, subthreshold

## I.INTRODUCTION

Supply voltage scaling is among the most efficient ways to reduce the power consumption of digital circuitry due to the quadratic relationship between dynamic power consumption and supply voltage. This technique will however degrade the performance due to the inverse relationship between circuit delay and the current level. As a consequence the threshold voltage in deep submicron processes is lowered to mitigate this problem. Decreasing the threshold voltage causes an exponential increase in subthreshold current enabling the possibility of utilizing this region for evaluating logic circuits with reasonable noise margins. Without applying special techniques subthreshold operation results in reduced speed due to the reduced evaluation current. The evaluation current in this case is the current flowing when the voltage of gate to source is less than or equals threshold voltage and the supply voltage is near the threshold voltage. As can be observed in Fig. 1, the Ion (when the transistor is evaluating) to Ioff (when the voltage of gate to source equals zero or is close to zero) ratio is low compared with the Ion/Ioff ratio for higher supply voltages. However, for ultra low power applications like implants and wireless sensor nodes, operating speed is not the primary concern since the demands for signal bandwidth are most often relaxed. For these applications the most important design goal is to optimize for low power consumption. The addition of 2 bits (A and B) with input carry (Cin) generates the SUM bit and the output carry bit ($C_{out}$). The following equations describe the full adder operation:

$SUM=A\oplus B\oplus C_{in}$ (1)

$C_{out}= (A.B) + (A.C_{in}) + (B.C_{in})$ (2)

$H= A\oplus B$ (3)

$SUM= H\oplus C_{in}$ (4)

$C_{out}=A.H'+ C_{in}.H$ (5)

Most adder topologies are based on two XOR gates (one to generate H and H', and the other to generate the SUM output), and one MUX (to generate the $C_{out}$) [1]. In [1] different circuit topologies have been analyzed and simulated in different ranges of supply voltages. In general the reported circuits do not work properly for ultra low supply voltages. For low supply voltages they suffer from a high delay because of the reduction in evaluation current

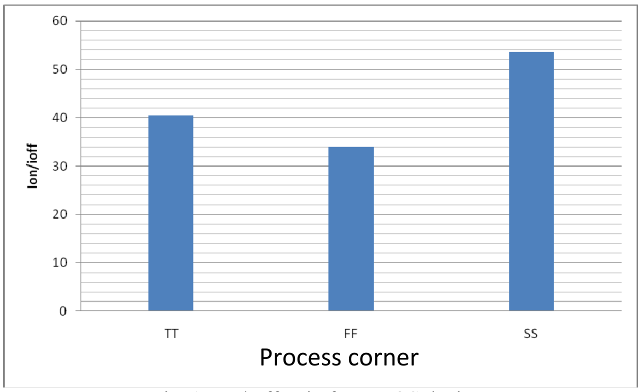


Fig. 1. Ion/Ioff ratio for NMOS devices

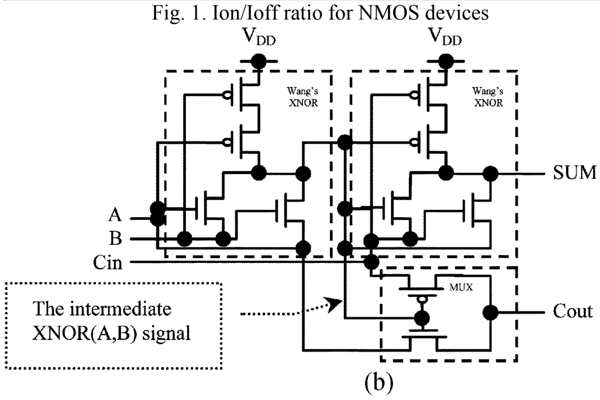


Fig. 2. SERF 1-Bit Full Adder[2]

charging/discharging the nodes in the circuit. A reduction in the evaluation current increases the circuit delay which again decreases the maximum frequency of the applied signals. Most of the proposed circuits in [1] are designed for high speed applications and small size in technologies before 0.18 micron and fail to work for supply voltages below 0.2 volt in 65nm CMOS technology mainly due to the many leakage mechanisms associated with nanoscale technologies.

Another proposed circuit is illustrated in Fig. 2. The Static Energy-Recovery Full adder (SERF) topology uses only 10 transistors which is the least number of transistors reported. The SERF is also considered to be the best in terms of power consumption, according to [2]. However for low supply voltages the circuit has a problem in the state when A=1, B=1, and Cin=0. In this case Cout goes to high using a NMOS pass transistor. But, it cannot be charged to VDD because of using NMOS to connect to VDD and also the gate of NMOS pass transistor is connected to VDD-Vth in this condition. So, Cout can rise just to VDD-2Vth that causes a constraint to work in ultra low supply voltages. For instance to avoid the failure with these inputs, suppose that Vth for NMOS transistor in 65nm is 0.18V, so Cout can rise only to VDD-0.36. Therefore, the supply voltage must be higher than 0.72V. Though, it depends on transistors sizing.With higher sized transistors, we can reduce the

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supply voltage more. VDD must be higher than Cout to have a high logic at the output. But by using an NMOS to charge Cout to high, causes it to fail for some cases, especially while the performance is more important. In [3] a 14-transistors full adder has been proposed. These different proposed circuits are all low power designs but they are not working properly in ultra low power applications when the supply voltage is decreased below the threshold voltage. Some of them have lower area compared to other standard circuits [4] but during the change of state in input signals, the voltage drop is irrefutable. Meanwhile to evaluate these circuits upsizing the transistors are required resulting in an increased power consumption. Reference [5] also proposes different configurations for full adder design in subthreshold region. However, these circuits also have some area overhead and do not work properly in ultra deep submicron technologies.

As shown in Eq. 1, the SUM signal may be generated using two XOR gates. The output of the first XOR-gate is the H signal that may be used to generate the COUT signal [6]. To implement the H signal and the SUM, XOR gates may thus be used, and for generating COUT from H, a small MUX 2X1 is used. As a consequence the most important and dominating part of the FA circuit is the XOR gate. Thus by designing an ultra low power XOR gate, an ultra low power FA is also feasible. In the following section different XOR circuit topologies are analyzed and then our proposed circuits are presented.

In the introduction the motivation for this work was presented along with an analysis of previously proposed FA circuits. In section II, the main building block of the FA, the low power XOR gate is described, analyzed and simulated. Also this section presents a low power XOR gate topologies designed for ultra low supply voltages in deep submicron technologies along with simulation results of the XOR gates. In section III, 1-bit FA design, using proposed XOR gates are presented. Finally conclusions are included in section IV.

## II.PROPOSED XOR CIRCUIT

Fig. 3 illustrates a XOR-XNOR gate for ultra low power applications [5]. This XOR-XNOR gate consumes very low power and also has a low leakage, but during the switching the drop in voltage at the outputs is inevitable. Another problem is the high area overhead since 16 transistors are employed in this circuit. In nanometer scale and also in subthreshold voltage this circuit cannot operate properly because of the many leaky NMOS transistors.

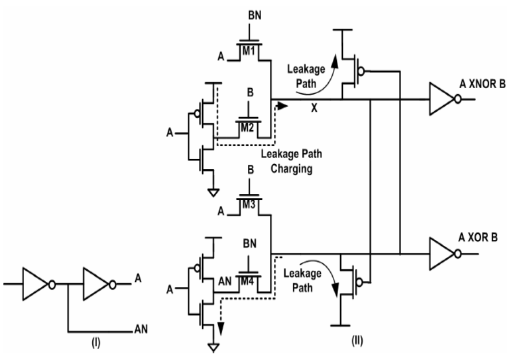

Fig.3. XOR-XNOR gate circuit [5]

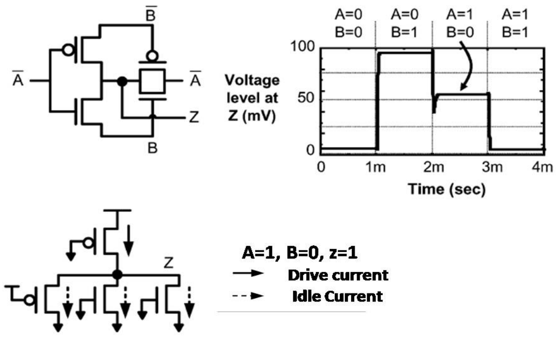

Fig.4. XOR gate and its operation [4]

During the inverter delay for generating the B’ and A’ signals an undesired voltage drop occurs. For solving the leakage paths in this circuit, the author has proposed using multi threshold voltage transistors as a suitable but expensive method due to the need for more process options. Other XOR gate circuits have been proposed in [4]. Fig 4 shows the standard XOR gate using static

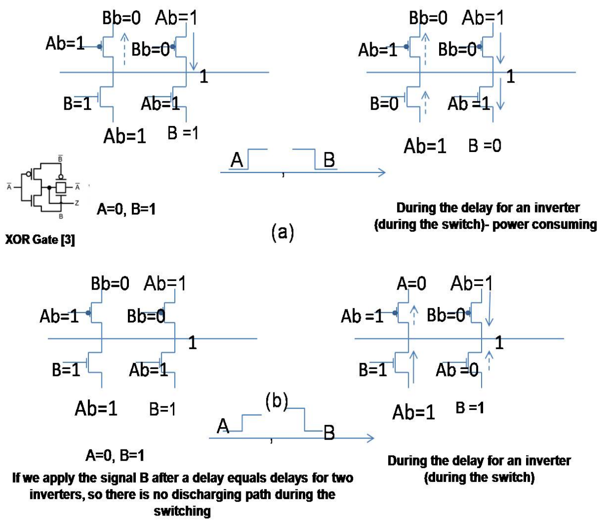

Fig.5. XOR behaviour during the switching from AB=”10” to AB=”01”

CMOS and pass transistor logic. The problems of these circuits have been explained in [3].

To solve the problem of leakage paths during the switching form AB=”01” to AB=”10”, an XOR gate in Fig.5 is proposed. The leakage occurs when the idle current of the parallel devices reduces the Ion/Ioff ratio. An example of leakage path is illustrated in the XOR gate in Fig. 5(a), (b), which shows the schematic of the tiny XOR gate [4] commonly used in traditional circuit design. An analysis of the drive currents and leakage currents for the input vector (A=0 , B=1) shows that since there are three ‘off’ devices and one ‘on’ device during this state, Ion/Ioff is degraded. The simulation shows that the output voltage is driven to Vdd but during the switching state there is a drop in output voltage that causes failure for supply voltage lower than 0.2V. This effect is further compounded if process variations are considered in the analysis.

Fig. 6 describes the circuit in state A=0, B=1 for XOR gate in [3]. The behaviour of this circuit is analysed during