A Perspective on Symmetric Lateral Bipolar Transistors on SOI as a Complementary Bipolar Logic Technology

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***Abstract*— Recently published reports suggest that symmetric lateral bipolar transistors on semiconductor-on-insulator (SOI) is CMOS compatible in fabrication process, and can be much denser than CMOS due to their much larger (5 to 10x larger) drive-current capability. When used in traditional bipolar circuits, SOI bipolar offers much lower power dissipation and/or much higher maximum speed. With both NPN and PNP devices of comparable characteristics, SOI lateral bipolar suggests the possibility of complementary bipolar (CBipolar) circuits in configurations analogous to CMOS. In this paper, the performance vs. power dissipation of CBipolar circuits is examined using analytic equations. It is shown that for CBipolar to be superior to CMOS in both performance and power dissipation, narrow-gap-base heterojunction structures, such as Si emitter with Ge base or Si emitter with SiGe base, are required.**

Index Terms— CBipolar, Complementary bipolar, SOI bipolar, symmetric lateral bipolar

I. Introduction

THE idea of a symmetric lateral Si-on-insulator (Si-OI) bipolar transistor with a self-aligned base contact located on top of the intrinsic-base region, and base widths of about 2 μm, was first demonstrated almost thirty years ago [1]. With lithography capability now at 22 nm in manufacturing, it is possible to fabricate both NPN and PNP Si-OI lateral bipolar transistors (Fig. 1) with base widths much less than 100 nm using CMOS-like processes [2]. Measured data show that Si lateral bipolar devices have drive-current capability much higher than CMOS [3, 4], while model studies suggest that they are scalable in lateral dimensions like CMOS and could have f_{max} > 1 THz [5].

The emitter/collector symmetry makes SOI lateral bipolar transistors immune to base push out (into the collector region) and suitable for circuits that involve operation in deep saturation or in both forward-active (emitter–base diode forward biased) and reverse-active (collector–base diode forward biased) modes. The result is significantly reduced power supply voltage for conventional bipolar circuits, and the possibility of complementary bipolar (CBipolar) inverters (Fig. 2) operating with a power supply voltage *Vcc* equal to the emitter–base forward bias voltage, V_{BE}, needed to achieve the target on current for the circuit.

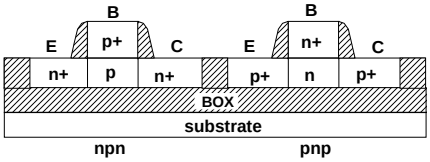

Fig. 1. Schematic illustration of the structure of complementary symmetric lateral bipolar transistors on SOI. (After [2])

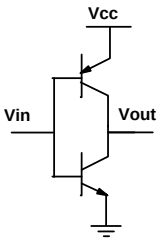

Fig. 2. Circuit schematic of a CBipolar inverter.

The operation of CBipolar inverters built using the transistor structure in Fig. 1 has been demonstrated experimentally [2, 3], and the concept of CMOS-like CBipolar circuits has been around for a long time [6]. It is an objective of this paper to develop insights into the operation of CBipolar circuits, using analytic current equations appropriate for SOI symmetric lateral bipolar transistors [4, 5]. Another objective is to examine the performance and power dissipation characteristics of CBipolar inverters, to see if CBipolar has the potential as an attractive digital circuit technology.

II. Symmetric Lateral Bipolar Transistors on SOI

As will be shown in Section III below, the ideal bipolar transistor characteristics for CBipolar applications are high on current (collector current) at low power supply voltage (*Vcc*), negligibly low off current at standby (V_{BE} = 0 and V_{CE} = *Vcc*), and very large current gain (β >> 100) when the transistors are turned fully on (at V_{BE} = *Vcc*). So far CBipolar (integrated NPN and PNP) has been reported only for Si-OI [2-4]. In this section we examine the properties of SOI lateral bipolar transistors as they apply to the operation of CBipolar circuits, using the reported data to illustrate both the status of CBipolar technology as well as the direction for future technology development. Several assumptions about the transistors are needed to make modeling using analytic equations tractable.

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These assumptions are discussed and clearly stated as they are made.

A. *Typical Integrated Si-OI NPN and PNP*

Figures 3 and 4 show the Gummel plots for typical integrated Si-OI NPN and PNP devices with E/C regions formed by As or B implantation. Both devices show ideal currents (varying at 60 mV/decade) for voltages up to about 0.9 V. The current saturation at larger voltage is due to a combination of high-injection effect and parasitic resistances [4]. The PNP currents clearly saturate at a lower level than those of the NPN. This is due to the fact that doping by boron implantation results in a more graded E/C junction and higher E/C series resistance for the PNP device. From device physics considerations, a PNP device and an NPN device having the same doping profile should have about the same *I–V* characteristics. In the following, we focus our discussion on the NPN *I–V* characteristics (Fig. 3), and simply ***assume that comparable PNP devices will be available***.

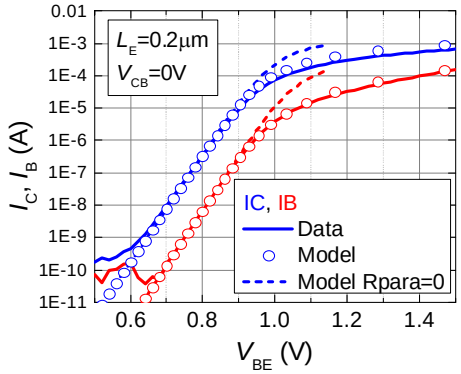

Fig. 3. Typical Si-OI NPN device. The device has T_{si} = 60 nm and N_E = N_C = 4E20/cm^3 formed by As implantation. The model currents were calculated using measured value of r_e = 267 Ω (see Fig. 7 for transistor equivalent circuit). Dash lines show calculated intrinsic device currents with no parasitic resistance. (After [4])

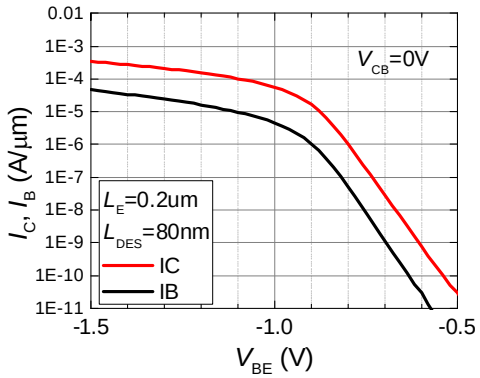

Fig. 4. Typical Si-OI PNP device. The device was integrated with the NPN in Fig. 3, and has N_E = N_C = 4E20/cm^3 formed by B implantation. (After [4])

In CBipolar inverter operation, the transistor in the off state is biased with V_{BE} = 0 and V_{CE} = *Vcc*. Fig. 5 is a plot of current as a function V_{BE} at fixed V_{CE} for the same NPN as in Fig. 3. It shows an off current of 0.1 μA/μm at V_{CE} = 1.0 V, increasing with V_{CE} to 0.7 μA/μm at V_{CE} = 1.5 V. Such levels of off current are comparable to those of state-of-the-art high-performance CMOS, but much too high for applications where low standby power is critical.

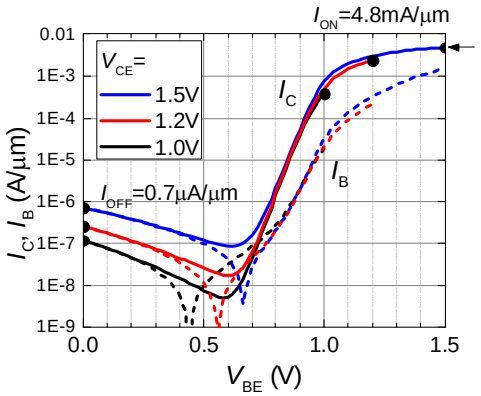

Fig. 5. Current characteristics for the same NPN as in Fig. 3 taken at fixed V_{CE} of 1.0, 1.2 and 1.5 V. (After [4])

The off currents at V_{BE} = 0 in Fig. 5 are caused by the leakage current in the reverse-biased B-C diode, as evidenced by the negative base current being equal to the collector current. Fortunately, reverse-bias diode leakage current is a function of the diode fabrication process. It is possible to obtain B–E and B–C diodes with negligible reverse-bias leakage currents. As an example, Fig. 6 shows the measured off current (i.e. collector current as a function of V_{CE} taken at V_{BE} = 0) of a Si-OI NPN device designed to have low off current. Figure 6 suggests an off current, including current due to instrument noise, of about 10 pA/μm at V_{CE} = 1.0 V. Such small off currents are low even by CMOS standards. Also, as will be shown later in Section III-B, such small device off currents can be ignored in consideration of the operation of CBipolar standby power dissipation. Therefore, in the rest of this paper, ***device off currents are assumed to be negligible and ignored completely***.

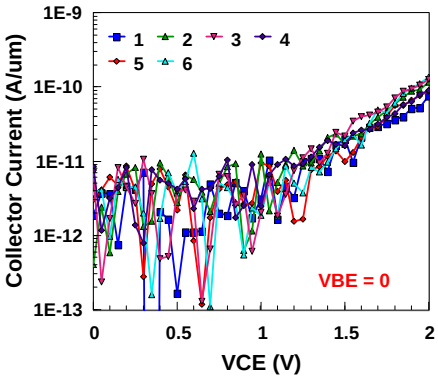

Fig. 6. Measured collector current per unit of L_E at V_{BE} = 0 as a function of V_{CE} for NPN transistors fabricated in the same experiment as those in Figs. 3 and 5, but using an E/C process designed to reduce B-E diode and B-C diode leakage current. The off current, including instrument noise, is 10 pA at V_{CE} < 1.0 V.

The measured base current in Fig. 3 behaves ideally, increasing with V_{BE} at 60 mV/decade, starting at less than 100 pA. The measured base current in Fig. 4 behaves ideally starting at less than 10 pA. The 60-mV/decade behavior indicates that the measured base current is the intrinsic base