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A novel ADPLL design using successive approximation frequency control

H. Eisenreich, C. Mayr, S. Henker *, M. Wickert, R. Schüffny

Circuits and Systems Laboratory, University of Technology Dresden, Dresden, Germany

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ABSTRACT

This paper presents a hardware implementation of a fully synthesizable, technology-independent clock generator. The design is based on an ADPLL architecture described in VHDL and characterized by a digital controlled oscillator with high frequency resolution and low jitter. Frequency control is done by using a robust regulation algorithm to allow a defined lock-in time of at most eight reference cycles. ASICs in CMOS AMS 0.35 μm and UMC 0.13 μm have been manufactured and tested. Measurements show competitive results to state-of-the-art mixed-signal implementations.

1. Introduction

The fast creation of complex system on chip (SoC) designs consisting of several intellectual property (IP) cores is state of the art for standard digital functionality [1]. A problem in this context are mixed-signal subblocks within the chip. These are highly technology dependent and a time-consuming re-design is necessary when technology or application area are modified [2].

An essential part of most modern digital circuits is a clock generator. This could be used to generate a high working frequency out of a much lower reference. It is also possible to regulate this output frequency dynamically with regards to low power design. The usage of a phase locked loop (PLL) architecture is a very effective way to form this function block. A PLL tries to synchronize a reference frequency with the output frequency of an oscillator by adjusting the latter.

Classical PLL implementations rely on analog components [1]. Because of this they are not suited for usage as an IP core. As mentioned above an extensive re-design has to be done any time the technology or the frequency specification is changed. A new approach is all-digital PLLs (ADPLL). Their hardware implementation consists completely of digital standard cells [1,2]. The phase detector, loop filter and frequency divider can easily be described in a high level hardware description language (HDL) to form a technology-independent softcore [1–3]. More difficult to implement is the digital controlled oscillator (DCO). The DCO designs presented in [1,4] still require a time-consuming manual fine tuning depending on the target library to meet the specified frequency and jitter specification. Compared to that, the clock generator design presented in this paper could be implemented in the same fast and easy way as a typical IP core in every standard digital synthesis-based design flow. This is realized by a combination of the standard-cell-based low jitter DCO presented in [3,5] and a robust frequency regulation algorithm based on successive approximation, as described in the following.

2. ADPLL concept description

The main application of such an ADPLL will be in supplying a clock reference for distributed digital processing systems on an SoC, based on one master reference clock. This design target necessitates a very high accuracy with respect to the master clock.

2.1. Architecture

The ADPLL is based on an architecture documented in a recent patent [5]. Long-term frequency stability and fine tuning of the output signal is achieved via switching between two adjacent lengths using a fractional divider (here called modulo *M* unit). Analytical jitter descriptions of this architecture have been derived in Ref. [3].

Since the clock is intended for digital processing systems, no analog fine tuning of the DCO delay elements is required. Besides long-term accuracy, the only additional requirement is that the jitter is small enough with respect to the clock period not to violate timing constraints of digital circuits supplied by this clock. This can be assured by using fast single elements in the DCO chain, where switching between two adjacent lengths does not substantially alter the basic clock period (Fig. 1).

* Corresponding author. Tel.: +49 351 463 34943.
E-mail addresses: eisenrei@iee.et.tu-dresden.de (H. Eisenreich), mayr@iee.et.tu-dresden.de (C. Mayr), henker@iee.et.tu-dresden.de (S. Henker), wickert@iee.et.tu-dresden.de (M. Wickert), schueffn@iee.et.tu-dresden.de (R. Schüffny).

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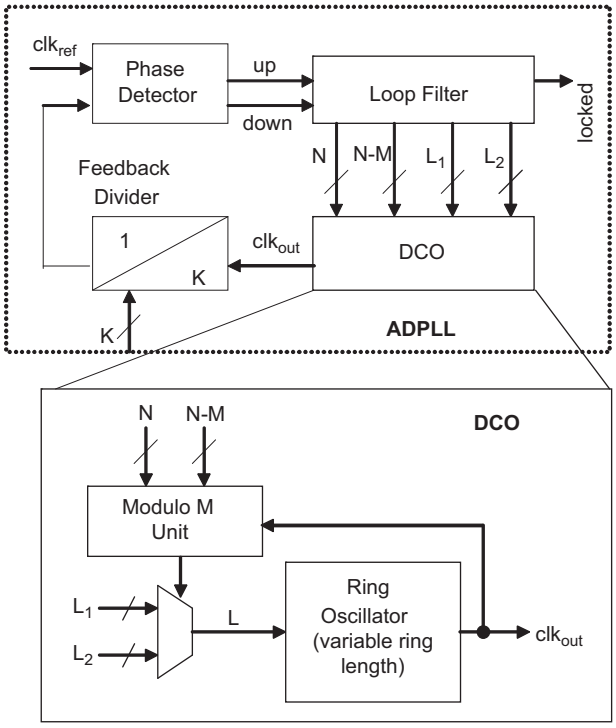

Fig. 1. Architecture of the discussed ADPLL.

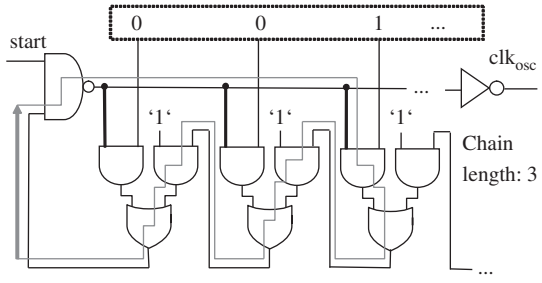

Fig. 2. Oscillator chain for a one-hot coded length of three.

As shown in Fig. 2, the DCO chain consists of AND–OR combinations which can be easily set to a defined chain length via a one-hot coded configuration word and have low propagation delay [3,6], in our case typically 80 ps for an AND–OR in 0.13 μm, respectively, 290 ps in 0.35 μm. When taking into account a factor of 2 for a full clock cycle (i.e. a high–low and a low–high transition), this compares well with the measured delays as shown in Figs. 17 and 18.

The basic building blocks as detailed above are the same for both presented implementations of the PLL. Compared to the 0.35 μm PLL, the 0.13 μm PLL has been designed for a higher clock reference, so the maximum multiplication factor of the feedback divider has been reduced. Additionally, the 0.13 μm PLL features a programmable output frequency divider that can be programmed independent from the feedback divider, thus allowing a wider frequency range of the output clock.

2.2. Functional description

In extension of the patented features [5], the architecture presented here is characterized by a technology independent, successive approximation type DCO frequency acquisition, with coarse tuning of the ring length and subsequent fine tuning of the fractional divider ratio (see Fig. 3).

Usually, the target frequency will correspond to an intermediate chain length between two discrete lengths L1 and L2. Once this chain interval has been found according to the procedure in Fig. 3, a similar successive approximation is used to find the ratio N/M of the modulo M unit (see Fig. 4).

If the regulation is down to switching the last bit of N, the PLL has achieved a lock on the frequency. The DCO is adjusted with both rising and falling edges of the reference clock, resulting in a lock acquisition of less than eight reference cycles. Once the fine trim is achieved, two adjacent chain lengths L1 and L2 have been selected, which are closest to the target frequency. The appropriate ratio of the usage of those chain length by the ring oscillator to ensure overall accuracy of the output frequency is determined by the modulo M unit.

The modulo M unit is central to the idea of long-term accuracy of the PLL output with respect to the reference clock. Since it governs the fine tuning of the output clock frequency and its working is entirely digital and thus free of error, relative clock accuracy can be extended arbitrarily by increasing the counter length of the modulo M unit. The only penalty of this extension is the increased lock time of the fine trim as shown in Fig. 4.

As denoted by the continued switching of the last bit of N in Fig. 4, the frequency regulation is continually active, ensuring a fast lock re-acquisition if the lock on a target frequency is lost (e.g. through temperature variations which may affect DCO delay times). The concept for this lock re-acquisition on the target frequency is a stepwise re-adjustment of both the fine trim and

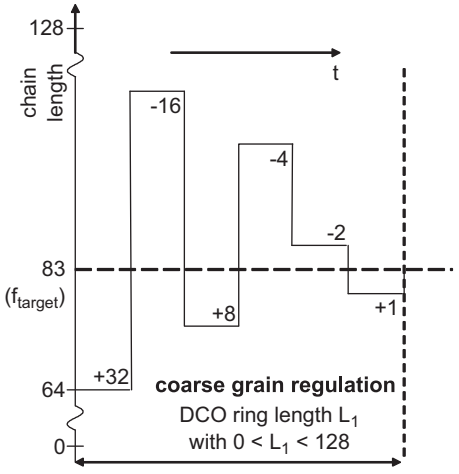

Fig. 3. Frequency acquisition and control scheme of the ring length tuning.

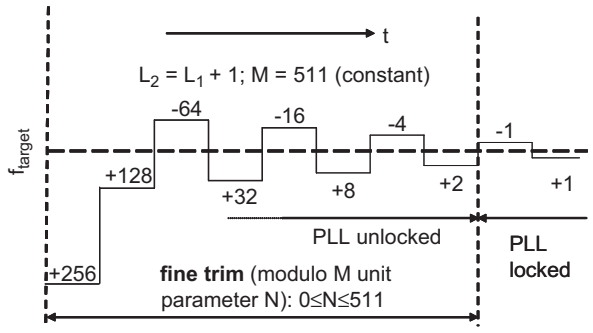

Fig. 4. Frequency acquisition and control scheme of DCO.