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New CCII-based versatile structure for realizing PID controller and instrumentation amplifier

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ABSTRACT

In this paper, a novel two-input two-output current-mode (CM) circuit for providing proportional-integral-derivative (PID) controller and instrumentation amplifier (IA) responses, depending on the passive component selection, is presented. The developed circuit uses only grounded capacitors (PID controller selection) and only grounded resistors (IA choice); accordingly, it is convenient for integrated circuit (IC) fabrication. The proposed new configuration can simultaneously realize both gain variable non-inverting and inverting responses without requiring extra additional components. The proposed topology for providing high output impedance currents can be easily cascaded with other CM structures. Finally, some time domain and frequency domain analysis with SPICE simulation program and experimental results are included to show workability and effectiveness of the proposed circuit.

1. Introduction

The use of current-mode (CM) realizations provides better properties when compared to that of their voltage-mode (VM) counterparts, as stated before in [1–3]. Moreover, subtraction and addition process is easy in CM implementations. A circuit using only grounded capacitors in integrated circuit (IC) has some important advantageous [4–7] because it is easy to implement in IC technology. Moreover, if controlled resistors are replaced instead of corresponding resistive components of a circuit, grounded controlled resistors use less number of transistors in contrast to floating ones.

The proportional-integral-derivative (PID) controllers are widely used in several control systems. Recently, they have been realized with two to three plus-type second-generation current conveyors (CCII+s) and five to six passive components [8,9]. Additionally, PID controller of [10] providing only VM transfer function (TF) is composed of four current differencing buffered amplifiers (CDBAs), eight resistors, a grounded capacitor and a floating capacitor.

On the other hand, in the open literature, a number of VM instrumentation amplifiers (IAs) have been reported [11–14]. The circuits in [11,12] employ two CCII+s, one floating and one grounded resistor. The resistors in the topology of [11] are eliminated by using controlled current conveyors (CCCIIs) instead of CCIIs as reported in [13]. Also, a topology similar to the one in [11] is reported in [14] by using operational floating current conveyors (OFCCs) instead of CCII+s and employing additional feedback resistors. However all of the above-mentioned circuits operate in VM, i.e. both input and output signals are voltage.

In this paper, a new two-input two-output CM versatile structure for realizing PID controller and instrumentation amplifier responses is proposed. It consists of only grounded capacitors (PID controller selection) and only grounded resistors (IA choice); thus, it is suitable for IC process. The presented PID controller depending on the passive component selection provides high output impedance currents resulting in easy cascadability with other CM circuits. All the parameters of the introduced PID controller can be chosen arbitrarily. Contrary to CM PID controllers of [8,9], the proposed one can simultaneously realize both inverting and non-inverting TFs. When compared to previously published IAs of [11–14], the suggested IA is CM, i.e. both input and output signals are current. Nevertheless, the developed IA selection requires a single passive component matching constraint. Computer simulations performed by means of SPICE program and experimental results are included to show the performance and effectiveness.

2. Proposed versatile circuit

The circuit symbol of the dual output CCII (DO-CCII) is given in Fig. 1. Using standard notation, DO-CCII ideally defined by $I_y=0$,

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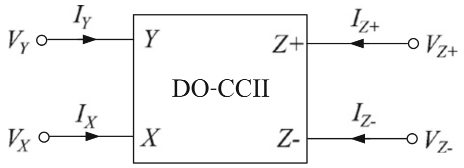

Fig. 1. Circuit symbol of the DO-CCII.

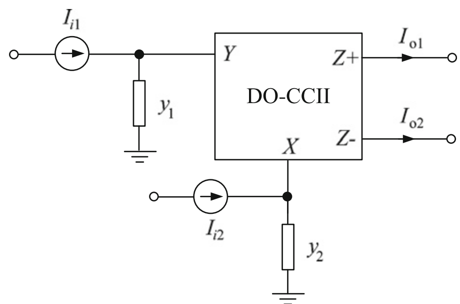

Fig. 2. Proposed current-mode PID controller and instrumentation amplifier topology.

$V_x = V_y$, $I_{z+} = I_x$ and $I_{z-} = -I_x$, can be practically characterized by the following matrix equation:

$$\begin{bmatrix} V_x \\ I_{z+} \\ I_{z-} \\ I_y \end{bmatrix} = \begin{bmatrix} \beta & R_x + sL_x & 0 & 0 \\ 0 & \alpha & sC_{z+} + 1/R_{z+} & 0 \\ 0 & -\gamma & 0 & sC_{z-} + 1/R_{z-} \\ sC_y + 1/R_y & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_{z+} \\ V_{z-} \end{bmatrix} \tag{1}$$

Here, the frequency dependent non-ideal current gains, α and γ, and voltage gain, β are ideally equal to unity. In addition, R_x, L_x, C_{z+}, C_{z-} and C_y are ideally equal to zero while R_{z+}, R_{z-} and R_y are ideally infinity.

The introduced circuit depicted in Fig. 2 always has $a > 0$, $I_{i2} = aI_{i1}$ and $I_{o2} = -I_{o1}$, and generates the following TFs:

$$H_1(s) = \frac{I_{o1}}{I_{i1}} = \frac{y_2}{y_1} - a \tag{2a}$$

$$H_2(s) = \frac{I_{o2}}{I_{i1}} = -H_1(s) \tag{2b}$$

Note that the introduced circuit can simultaneously realize both non-inverting and inverting responses, which increases the flexibility of the proposed one. If non-ideal gains of the DO-CCII are considered, the TFs of (2) are convert to

$$H_1(s) = \frac{I_{o1}}{I_{i1}} = \alpha\beta\frac{y_2}{y_1} - a \tag{3a}$$

$$H_2(s) = \frac{I_{o2}}{I_{i1}} = -\beta\gamma\frac{y_2}{y_1} + a \tag{3b}$$

If parasitic impedances of the DO-CCII are considered, the TFs of (2) turn into

$$H_1(s) = \frac{I_{o1}}{I_{i1}} = \frac{y_2/(y_2(sL_x + R_x) + 1)}{y_1 + sC_y + (1/R_y)} - a \tag{4a}$$

$$H_2(s) = -H_1(s) \tag{4b}$$

In (4a), the loading effect is ignored, i.e. outputs are connected to ground.

The implementation of the input currents for the proposed circuit is given in Fig. 3, where a CCII with two Z− terminals is employed. The multiplier constant a can be easily realized by changing aspect ratios of MOS transistors. Alternatively one can use electronically tunable current conveyor (ECCII) [15] instead of CCII in Fig. 3 to adjust the parameter a by means of an external current.

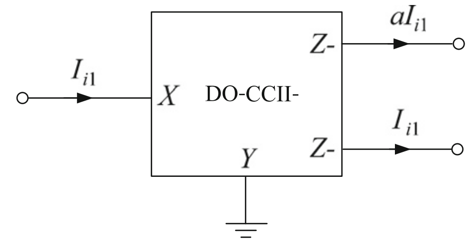

Fig. 3. Realization of input currents of the proposed circuit using a CCII.

2.1. PID controller

If $y_1 = 1/(1/(sC_1) + R_1)$ and $y_2 = sC_2 + 1/R_2$ are chosen in Fig. 2, the following TF can be obtained:

$$H_k(s) = K_{pk} + \frac{1}{sT_{ik}} + sT_{dk} \tag{5}$$

In (5) ($k = 1, 2$), the proportional gain (K_p), the integral time constant (T_i) and the derivative time constant (T_d) parameters of the proposed PID controller are evaluated as

$$K_{p1} = \alpha\beta\left(\frac{R_1}{R_2} + \frac{C_2}{C_1}\right) - a \tag{6a}$$

$$K_{p2} = -\beta\gamma\left(\frac{R_1}{R_2} + \frac{C_2}{C_1}\right) + a \tag{6b}$$

$$T_{i1} = \frac{C_1 R_2}{\alpha\beta} \tag{6c}$$

$$T_{i2} = -\frac{C_1 R_2}{\beta\gamma} \tag{6d}$$

$$T_{d1} = \alpha\beta C_2 R_1 \tag{6e}$$

$$T_{d2} = -\beta\gamma C_2 R_1 \tag{6f}$$

It is observed from equations in (6) that T_d and T_i can be controlled through R_1 and R_2 for fix valued capacitors, respectively. Further, K_p can be adjusted via multiplier constant, a, which can be controlled externally using ECCII [15]. The active and passive component sensitivities with respect to parameters of the PID controller T_d, T_i and K_p are no more than unity in magnitudes. The resistors of the realized PID controller R_1 and R_2 can be tuned electronically by respectively replacing a CMOS technology based floating tunable resistor [16] and a CMOS technology based grounded one [17].

2.2. Instrumentation amplifier

If $y_1 = 1/R_1$ and $y_2 = 1/R_2$ are chosen in Fig. 2, the following instrumentation amplifier responses are obtained as follows:

$$I_{o1} = \alpha\left(\frac{\beta R_1}{R_2} I_{i1} - I_{i2}\right) \tag{7a}$$

$$I_{o2} = -\left(\frac{\beta R_1}{R_2} I_{i1} - I_{i2}\right)\gamma \tag{7b}$$

Here, α and γ are current gains defined before, which can be set any value by changing aspect ratios of the CMOS transistors. From (7a), the differential-mode gain (A_{dm}), common-mode gain (A_{cm}) and common-mode rejection ratio (CMRR) are respectively