Microelectronics Reliability 54 (2014) 1489–1499

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Introductory Invited Paper

HKMG CMOS technology qualification: The PBTI reliability challenge

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ARTICLE INFO

Article history:
Received 24 March 2014
Accepted 24 March 2014
Available online 10 May 2014

Keywords:
PBTI
High-k
Qualification
Charge trapping
HfO_2
Threshold voltage instability

ABSTRACT

We present a brief overview of Positive Bias Temperature Instability (PBTI) commonly observed in n-channel MOSFETs with SiO_2/HfO_2/TiN dual-layer gate stacks when stressed with positive gate voltage at elevated temperatures. We review the origin and present understanding of the characteristics of oxide traps that are responsible for the complex behavior of threshold voltage stability. We discuss the various physical mechanisms that are believed to govern the transient charging and discharging of these traps as the backbone of the models that have been proposed for PBTI degradation and recovery. Next we review the state-of-the-art in PBTI characterization and we present some of the key stress results on both the device as well the circuit level. Special emphasis is given on the open PBTI issues that need to be carefully addressed for a robust reliability methodology that accurately predicts PBTI lifetimes. Finally we mention some of the gate stack scaling effects on PBTI.

1. Introduction

High dielectric constant (high-k) materials were the subject of rigorous research in the beginning of the previous decade [1–6] as the most promising candidates to replace the conventional, reaching its physical limits, SiO_2-based gate dielectric and thus providing the means of further scaling CMOS technology in accordance to the International Technology Roadmap for Semiconductors (ITRS) [7]. It was demonstrated by many research groups that the use of a high-k material as the gate dielectric offers a significant reduction in gate leakage density because a physically thicker gate stack can be used at the same SiO_2 Equivalent Oxide Thickness, EOT [8–14]. This inherent to high-k suppression of gate leakage current allows for further EOT scaling below 1 nm, while maintaining acceptable gate leakage currents, and thus enables the traditional MOSFET gate length scaling which is central to the CMOS technology performance improvement. Several materials have been evaluated over the years, namely, hafnium, zirconium, aluminum. The semiconductor industry preferred high-k dielectric is HfO_2 based which was introduced in the 45 nm technology node [15] along with TiN as a metallic gate electrode to form the so called High-k/Metal Gate (HKMG) stack, exhibiting all the above mentioned advantages [16–18].

This recent impressive progress in the performance of HKMG transistors and the complicated nature of the multi layer gate material have brought to the forefront of High-k/Metal Gate technology development the issue of reliability and in particular the Positive Bias Temperature Instability (PBTI) [19–32]. Most of these studies showed a significant positive threshold voltage (V_T) shift for n-channel MOSFET's subjected to positive bias temperature stressing, which was attributed to the pre-existing electron traps (presumably oxygen vacancies in the high-k layer [33]). However, other authors have argued that voltage stress-induced defect generation may also contribute to the device V_T instability [27–32]. The effectiveness of the stress-induced trap generation in these gate stacks along with the time and voltage dependence of the PBTI induced device degradation still remain controversial issues with the conclusions varying with the applied measurement techniques, test conditions and the gate stack process details. Several review articles have recently been written, focusing on HKMG reliability issues including PBTI [34–37].

In this contribution, we summarize the recent progress in the understanding of various PBTI reliability aspects. We first discuss the various processes and underlying physical mechanisms of PBTI. Then we review the test and measurement procedures specifically tailored to capture the reliability aspects of these new gate stacks and we present some key PBTI stress results from the literature as well as our own experiments. The gate stack scaling effects on PBTI are also reviewed and some aspects of the PBTI effects on Ring Oscillator circuits are discussed. Finally, I have attempted to highlight the PBTI areas where there is uncertainty and will need continued attention in the near future within the context of technology qualification.

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http://dx.doi.org/10.1016/j.microrel.2014.03.018
0026-2714/

2. What is PBTI?

PBTI is an increase in the threshold voltage of n-channel MOSFET under a positive gate bias at elevated temperature. As a result of the threshold voltage shift, the drain current degrades but typically no mobility or transconductance degradation is observed. Similar to the NBTI case, PBTI induced threshold voltage shift (and current degradation) recovers fast as soon as the gate stress voltage is removed. The recovery is typically partial under small positive gate voltages but it can be complete under a sufficiently large negative gate bias. The electric field and temperature under which PBTI is activated are comparable to those leading to NBTI degradation in p-channel MOSFETs. PBTI is mainly attributed to transient charging–discharging of pre-existing (process induced) electron traps in the high-k layer. Although the exact physical and chemical nature of electron traps is still under rigorous research by the scientific community, there have been results of ab initio calculations [38,39] as well as experimental studies based on electron spin resonance (ESR) measurements [40] that point to oxygen vacancies as possible defects controlling threshold voltage instability. Furthermore, as we discuss below, trap characteristics obtained from time-resolved measurements and defect spectroscopic techniques have been found to match those of oxygen vacancy defects. The details of how PBTI occurs are not entirely clear, however. Next, we discuss some of the mechanisms of electron trapping–detrapping and the PBTI models that have been proposed.

3. Electron trapping–detrapping mechanisms and defect generation

In [19] Kerber et al. introduced a variant (amplitude sweep) of the charge-pumping (CP) technique [41] to quantitatively capture the transient charging phenomena responsible for the V_T instability in SiO_2/HfO_2 dual layer dielectrics. Based on the obtained electrical results, they proposed a simple model which postulates the existence of a defect band in HfO_2 layer located in energy between the silicon and hafnia conduction bands (area between dashed lines in Fig. 1). The rapid shift of the defect band's energy with respect to the Fermi level in the Si substrate as the gate bias varies from positive to negative bias drives the fast charging and discharging of the defects near the $SiON/HfO_2$ interface (dark shaded area, Fig. 1) by electron tunneling through the interfacial SiON layer.

The Amplitude sweep Charge Pumping (ACP) technique entails applying a trapezoidal pulse train of frequency f to the gate of the MOSFET under test where the low bias level (extraction voltage, V_{base}) is kept constant and the high bias level (injection voltage, V_{peak}) is varied. In this experiment and in view of the transient charging model discussed above, electrons are periodically injected from the Si inversion layer into the gate stack during the high bias part of the signal at V_{peak} (Fig. 1b) and then extracted to the Si substrate during the low bias phase at V_{base} (Fig. 1c). Fig. 2 shows a typical result obtained with this measurement where the solid symbols mark the number of pumped carriers (calculated from the time-averaged substrate current) for three different injection/extraction times, $t = 1/2f$ (50% duty cycle). It is seen that there is a rapid increase of the CP signal with V_{peak}, attributed to the charge exchange with the defects in the gate stack. The strong frequency dependence that is also observed reflects the fact that the charging is controlled by tunneling and that the amount of trapped charge depends on the charging time. The assumption that the defects that are being charged during this process reside in the HfO_2 layer is supported by the fact that the density of trapped carriers measured with the ACP technique is one order of magnitude higher than the density measured with the conventional base level sweep CP technique which measures interface states (inset of Fig. 2). Hence, the charge that is measured with the ACP measurement cannot be located at the $Si–SiO_2$ interface. The open symbols in Fig. 2 illustrate the de-trapping characteristics during a reverse amplitude sweep where de-trapping is observed to strongly increase (with increasing negative bias and time) eventually resulting in complete charge recovery.

Recently, Cartier et al. employed the ACP measurement in the reverse amplitude sweep mode and demonstrated that it can be used as a defect spectroscopic technique where the energy distribution of the electron traps can be extracted [42]. Their results suggested the presence of trap levels within 1.2 eV below the energy of the bottom of the conduction band of HfO_2 (see Fig. 6 in Ref. [36]) and in the vicinity of the Si substrate conduction band under flatband conditions, as postulated by the model discussed above (Fig. 1). These defect spectroscopic results are also consistent with the calculated energy levels for the various charge states of the oxygen vacancy in HfO_2 [39] further supporting the notion that PBTI is a direct consequence of charge exchange with an oxygen vacancy based defect band in HfO_2.

Besides the electron tunneling through the interfacial SiON layer as the process of fast charging and discharging of the HfO_2 defects, various other mechanisms have also been proposed. Fig. 3 illustrates three possible and competing with each other electron detrapping mechanisms under positive gate bias [43]. The mechanism 1 is a detrapping mechanism in the high-k layer and assumes

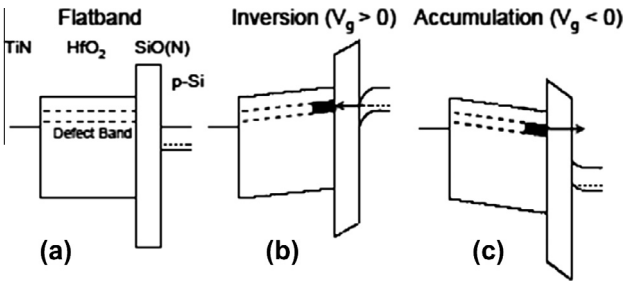

Fig. 1. Schematic energy-band diagram of a SiO_2/HfO_2/poly-Si gate stack containing a defect band in the HfO_2 layer at flatband condition shown in (a). For (b) positive and (c) negative bias, the defects located near the SiO_2 interfacial layer move rapidly with respect to the Fermi-level in the Si substrate. In schematic (b) electron traps are negatively charged and in schematic (c) electron traps are discharged (after Ref. [19]).

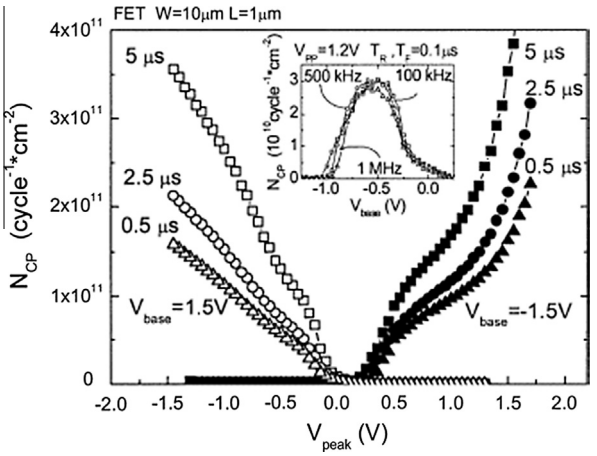

Fig. 2. Charge-pumping characteristics measured on n-channel MOSFET with a 3-nm deposited HfO_2 layer. The conventional base level sweep (inset) is compared with the amplitude sweep using constant base level (after Ref. [19]).