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A new write assist technique for SRAM design in 65 nm CMOS technology

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ABSTRACT

In this paper, a new write assist technique for SRAM arrays is proposed. In this technique, to improve the write features of the SRAM cell, a negative voltage is applied to one of the bitlines in the SRAM cell while another bitline is connected to a boosted voltage. Improved write features are attributed to the boosting scheme from both sides of the SRAM cell. This technique is applied to a 10T-SRAM cell with transmission-gate access devices. The proposed design gives 2.7×, 2.1× faster write time, 82% and 18% improvement in write margin compared with the standard 8T-SRAM cell with and without write assist, respectively. All simulations have been done in TSMC 65 nm CMOS technology. The proposed write assist technique enables 10T-SRAM cell to operate with 24% lower supply voltage compared with standard 8T-SRAM cell with negative bitline write assist. Due to the improved supply voltage scalability a 33% leakage power reduction is achieved.

1. Introduction

CMOS technology has been the cornerstone of semiconductor devices for years. Moore's law motivates the technology scaling in order to improve the performance features such as speed, power consumption and area. Although circuits and systems benefit from technology down-scaling in some aspects, the undesired features such as short channel effects (SCEs) and sensitivity to process variations are also consequential. The effect of process variations on performance is a key issue in scaled CMOS technology. This effect gets more pronounced as the size of transistors is reduced. One of the highly sensitive circuits to process variations is SRAM due to using extremely small devices in order to achieve high density. Process variations can be due to global or local mismatches between devices. Global mismatch refers to die-to-die variation in device and local mismatch refers to mismatch between transistors on the same die [1]. Local mismatch in SRAM devices can easily lead to read stability degradation (stored data is flipped during read), read failure (data is not read during read period), writeability decrease or write time increase. On the other hand, the trade-off between read and write operations makes it difficult to improve both simultaneously.

Fig. 1(a) shows the standard 6T-SRAM cell structure. It consists of two back to back inverters (PUL-PDL and PUR-PDR) that keep the data and its inverse on nodes Q and QB, respectively. The access transistors (ACL-ACR) are used to perform read and write operations. Due to using a common path (ACL-ACR) for read and write operations, improving the read stability will lead to degradation of the writeability of the cell and vice versa. To improve the read stability of an SRAM cell, beta ratio ($\beta = W_{PD}/W_{AC}$) can be increased, while lower alpha ratio ($\alpha = W_{PU}/W_{AC}$) is desirable to improve the cell writeability. Finally, during hold mode, equal strength for pull up and pull down transistors ($W_{PU} = W_{PD}$) sets the trip point of the two back-to-back inverters at $V_{SUPPLY}/2$ and ensures maximum noise margin.

Several solutions have been proposed in literature from device to architecture level to improve SRAM cell functionality. For instance, at the device level, using new devices such as FinFET, leads to significant SRAM performance improvement [1–5]. At the cell level, new cells such as 7T, 8T, 9T, 10T, and 11T [5–15] have been proposed that have resulted in a higher cell area. Among them standard 8T-SRAM cell shows a very good compromise between cell features improvement and cell area penalty [6]. Fig. 1(b) shows the standard 8T-SRAM cell. This cell consists of a 6T storage cell and a 2T read buffer which isolates read path from write path and storage nodes. In this way, read and write features can improve simultaneously. However, the write margin of the SRAM cell varies significantly due to the process variations of access transistors. This is due to the fact that the write current flows through the access transistors and corresponding variations will affect the write margin of the SRAM cell significantly. On the other hand, while reading the cell, the read

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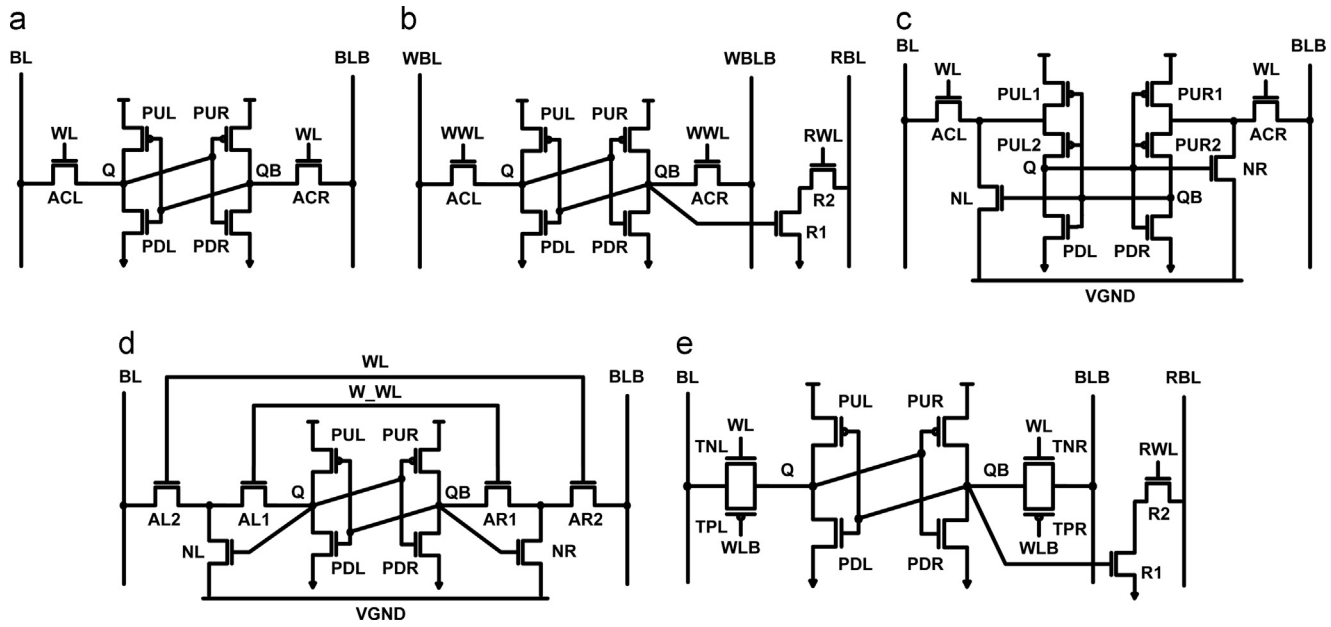

Fig. 1. (a) Standard 6T- (b) Standard 8T- (c) P–P–N 10T- [13] (d) 10T- [14] (e) TGA 10T-SRAM cells [15].

current flows through the read buffer (R1 and R2) which its variation does not affect read margin. As a result, the write margin is a key parameter especially in the scaled supply voltages which the effect of process variation is more pronounced. Supply voltage scaling is an effective way to decrease the power consumption of the System-on-Chips (SoCs). 10T-SRAM cells are mainly proposed to work in ultra-low voltages (near/subthreshold region). Fig. 1(c)–(e) shows three 10T-SRAM cell schematics. Lo et al. proposed a P–P–N 10T-SRAM cell in [13]. This cell is called P–P–N due to the fact that each of the cross-coupled inverters consists of three transistors cascaded in a P–P–N sequence as shown in Fig. 1(c). This cell shows a low cell leakage due to the three stacked transistors as inverter and it also has a good immunity to data dependent bitline leakage [13]. However, the use of stacked transistors limits supply voltage scaling. Fig. 1(d) shows another 10T-SRAM cell in the literature which uses two transistors in series as access device [14]. Utilizing two control signals (WL and W_WL) enables implementation of bit-interleaving structure. The main drawback of this cell is related to its weak writeability due to the cascaded access transistors which can limit the power supply scaling. Fig. 1(e) shows the Transmission-Gate Access transistor SRAM cell (TGA-SRAM) proposed in [15]. The transmission gate access devices are used to improve the writeability of the cell that improves the supply voltage scalability, as well. On the other hand, the read path is isolated from storage nodes that results in a high read noise margin. Single ended read sensing scheme will decrease the TGA-SRAM cell access time. However, utilizing pseudo-differential sensing improves the access time, significantly [16]. All in all, each of the 10T-SRAM cells has some pros and cons which mentioned above. However, comparing the cells is not the focus of this paper and we will use only one of the above mentioned cells in order to apply the proposed write assist technique.

At the architecture level, read and write assist techniques improve SRAM robustness and performance while occupying less area compared to the cell techniques (e.g. 8T and 10T) and can be used with any type of SRAM.

In this paper, a new write assist technique is proposed that improves SRAM writeability, significantly. This new technique applies a boosted voltage ($V_{DD}+\Delta V$) to the high-going bitline and a negative voltage on the low-going bitline simultaneously. This technique results in a significant improvement in Write Margin (WM) and Write Time (WT). In this technique, coupling capacitances are used to produce boosted and negative voltages.

In order to make Boosted-Negative Bit-Line (BNBL) technique more efficient, the TGA 10T-SRAM cell is used. Simulation results in 65 nm CMOS technology show 2.7 × and 2.1 × faster write time and 82% and 18% improvement in write margin compared with 8T-SRAM cell without and with write assist technique, respectively.

The remainder of this paper is organized as follows. In Section 2, a brief survey of existing write assist techniques is presented. In Section 3, the basic concept of the proposed BNBL technique is presented and validated by mathematical analysis. The efficacy of BNBL technique is shown in Section 4 through simulation results. Finally, the conclusions are drawn in Section 5.

2. State of the art

In this section, existing write assist techniques such as cell V_{DD} collapse, negative bit-line, boosted word-line and cell GND boost are discussed. The circuit implementation of the best technique amongst them (negative bit-line) is discussed with three examples.

2.1. Write assist techniques

In order to improve the write margin of SRAMs, several write assist techniques have been proposed. Some of these techniques rely on cell V_{DD} collapse [17–20], Negative Bit-Line (NBL) [21–25], Boosted Word-Line (BWL) and cell GND boost [26]. Negative bitline write assist circuit applies a small negative voltage ($-\Delta V$) instead of GND at the low-going BL. This negative voltage on BL increases the strength of the access transistor by increasing V_{GS} from V_{WL} to $V_{WL}+\Delta V$ (V_{WL} is the wordline voltage). Strengthening the access transistor without any effect on back-to-back inverters leads to improved writeability.

The BWL technique increases the word line voltage (V_{WL}) connected to the gate of access transistors (ACL and ACR in Fig. 1) during write operation. This increases the gate source voltage of access transistors ($V_{GS\text{-}ACL}$ and $V_{GS\text{-}ACR}$) and improves its driveability. Cell V_{DD} collapse and cell GND boost techniques improve the writeability of the cell by weakening the back to back inverters during write operation. However, these techniques degrade the