New configuration memory cells for FPGA in nano-scaled CMOS technology

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ABSTRACT

In nano-scaled CMOS technology, the reduction of soft error rate and leakage current are the most important challenges in designing Field Programmable Gate Arrays (FPGA). To overcome these challenges, based on the observations that most configuration bit-streams of FPGA are zeros across different designs and that configuration memory cells are not directly involved with signal propagation delays in FPGA, this paper presents three new low-leakage and hardened configuration memory cells for nano-scaled CMOS technology. These cells are completely hardened when zeros are stored in the cells and cannot flip from particle strikes at the sensitive cell nodes. These cells retain their data with leakage currents and positive feedback without a refresh cycle. Simulation results show that the proposed cells are working correctly during their configuration and idle cycles and that our cells have a lower soft error rate and leakage current in 22-nm as well as in 65-nm technologies.

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1. Introduction

Devices in CMOS technology have been scaled down aggressively with each technology generation to achieve a higher integration density and performance [1]. However, the leakage current has increased drastically with technology scaling and has become a major contributor to the total IC power [1]. Furthermore, as the feature sizes of devices and the supply voltage in CMOS technology were scaled down, the probability of soft errors increased. Soft errors are radiation-induced faults that occur because of a particle hit, either by an alpha particle from impurities in the packaging material or a neutron from cosmic rays [2].

Field-programmable gate arrays (FPGA) are ideal for implementing any type of digital system because they are reconfigurable and can be programmed to implement any digital logic [4]. Each FPGA involves an array of logic blocks that are connected through a network of routing switches that are all programmed by SRAM cells [4]. A six-transistor SRAM cell is conventionally used as the configuration memory cell [5]. As mentioned above, as the CMOS technology is scaled down, the total leakage current of chips increased. Furthermore, the total leakage current of a chip is proportional to the number of transistors on the chip, and because the configuration memory includes a large number of transistors on the FPGA chip, its leakage has also become a more

significant component of total chip leakage in scaled CMOS technology. In addition, in scaled CMOS technology, the supply voltage and the nodal capacitance are reduced. Thus, an important drawback of SRAM-based FPGAs is that these devices are susceptible to single event upset (SEU) errors caused by cosmic particle strikes [6]. Therefore, the soft error rate and the leakage current of a configuration memory cell are the two most important parameters in designing configuration memory cells for FPGAs in nano-scaled CMOS technology.

In response to the challenges of a conventional six-transistor SRAM cell, our objective is to develop a hardened SRAM cell with dual threshold voltage transistors to reduce the leakage current of the cell without significant area overhead. The rest of this paper is organized as follows. Section 2 describes the basic structure of an FPGA. Then, we propose new configuration memory cells in Section 3. Next, in Section 4, a particle strike to the new configuration memory cells is investigated. The leakage current of new configuration memory cells is investigated in Section 5. Section 6 explains a look-up table and routing switch based on the new cells. Section 7 presents a comparison with other related works. Finally, we summarize the key results in Section 8.

2. Background

Fig. 1 shows the basic and simple structure (island-style) of an FPGA [7]. As shown in the figure, each FPGA consists of an array of configurable logic blocks (CLB) and a network of routing switches. Each configurable logic block includes a cluster of lookup tables (LUT),

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and each lookup table includes a set of SRAM cells and a multiplexer, as shown in Fig. 2(a) [5]. Also, Fig. 2(b) shows a typical buffered FPGA routing switch [8]. Based on configuration data stored in SRAM cells, each input is routed to the output of the switch. Conventional six-transistor SRAM cell (CV 6T SRAM cell) is used as the configuration memory cell [5]. Fig. 2(c) shows circuit schematics of CV 6T SRAM cell.

The effect of SEU on SRAM-based FPGA can be classified into either a transient error or a permanent error [6,9]. SEUs can directly make tra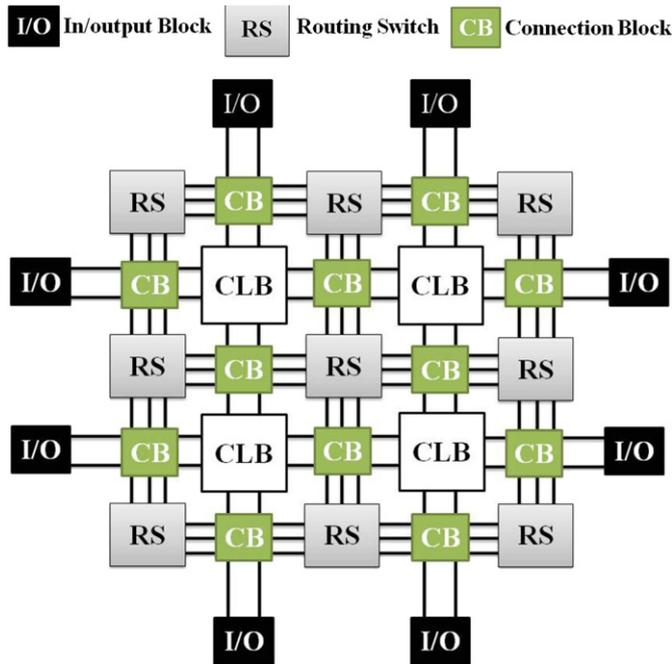nsient errors on memory elements and change the contents of register files and flip-flops. These errors are called transient because they may be overwritten or corrected using error-detection and correction techniques. Thus, transient errors impact the user-defined logic and flip-flops of the FPGA [9]. In addition, SEUs can make permanent errors on an FPGA if they alter the contents of the configuration bits [9]. In this case, the configuration bit remains erroneous until the new configuration is downloaded into the FPGA [6,9]. Furthermore, to accommodate the logic that implements reconfigurability, FPGA flexibility is achieved at the cost of silicon area occupation [10]. As technology has progressed, the area constraint has become less restrictive; however, the large number of integrated transistors is a source of higher energy consumption than ASICs [10].

It was observed in [11,12] that the configuration bit-stream of FPGA contains 87% zeros across different designs. The main reason for the higher number of zeros is the large unused number of the routing bits. Also in the case of an FPGA, it can be noticed that SRAM configuration memories are not directly involved with signal propagation delay [10]. In the next section and based on the observations that most configuration data are zeros and the propagation delay of configuring data into SRAM cell has not had any effect on FPGA performance, we designed low-leakage hardened cells that are resistant to flipping caused by a particle strike, either from 0 to 1 or from 1 to 0.

3. New cell

Fig. 3 shows an equivalent circuit to develop an eight-transistor configuration cell using a supply voltage of 0.95 V in a 22-nm technology node. Hereafter, we refer to this cell as 'basic new cell' or 'basic new configuration memory cell'. Also, Table 1 lists the sizes of transistors and threshold voltage level in both types of configuration cell. For fair comparison, the sizes of transistors in basic new cell are set to be the same as the improvement-leakage new cell, but in general, sizes of transistors in basic new cell can be different from sizes of transistors in improved-leakage new cell.
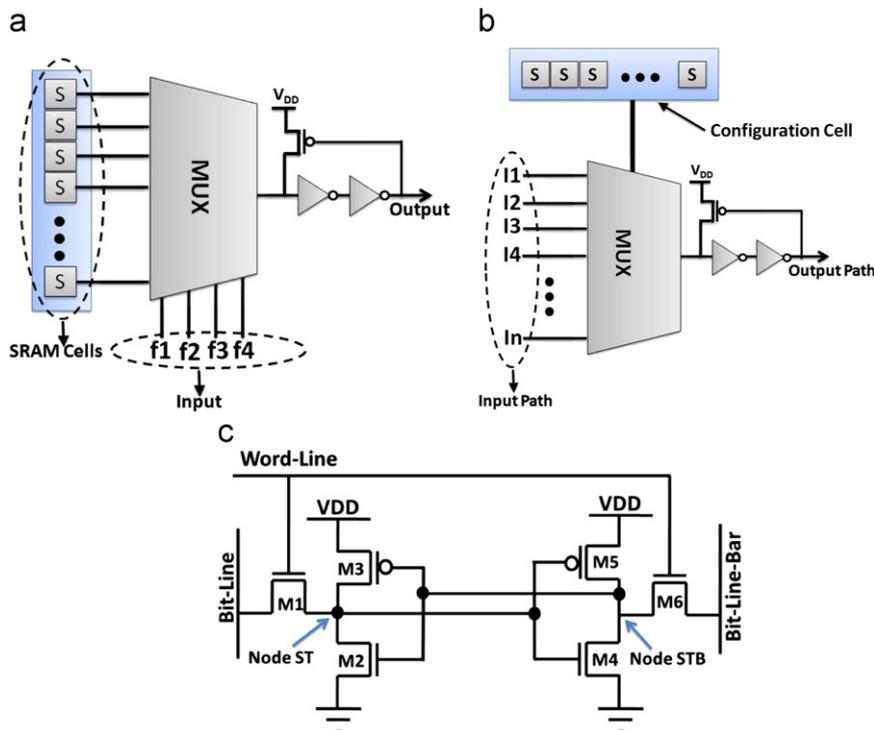

Fig. 1. Island-style architecture of an FPGA.

Fig. 2. (a) Structure of a Look-up Table (LUT). (b) Structure of a routing switch. (c) Circuit schematic of a convectional six-transistor SRAM cell (CV 6T SRAM cell).