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Ultrathin DPN STI SiON liner for 40 nm low-power CMOS technology

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ABSTRACT

At sub-40 nm CMOS technology nodes, the implementation of shallow trench isolation (STI) becomes more challenging due to shrinking geometries and stricter device leakage requirements. As device geometries are shrinking, STI liner is also becoming thinner and plays an important role for the minimal consumption of device active area while effectively rounding the STI corner and minimizing stress-induced defects. Consequently, STI stress is enhanced by the scaling of STI-pitch, the volume expansion induced by STI liner and film stress of filling materials. This paper discusses the benefits of SiON liner growth by decoupled-plasma-nitridation (DPN) and SiON liner induced stress compared to conventional pure oxide liner growth by in situ steam generation (ISSG). Thin STI SiON liner offers lower sub-threshold leakage current without drive current loss for transistor performance. Moreover, junction leakage current is also reduced with scaling device active area. Thus, better device performance results in better minimum operation voltage (Vcc_min) of low-power 6T-SRAM. This paper demonstrates the influences of thin STI SiON liner growth by DPN in STI manufacture.

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1. Introduction

At sub-40 nm device nodes, implementation of STI becomes more challenging, incorporating aspects of trench definition, liner oxidation, and trench fill with deposited oxide. The step following the trench etch is liner oxidation, which is important as it can adversely impact transistor performance if it is not implemented properly. Below 65 nm technology node, the major challenge in STI is managing the mechanical stress of STI on device active area [1,2]. In the STI process, the liner oxidation step is necessary to round the top and bottom trench corners. A better corner profile of STI near the active area can improve undesirable kink effect of parasitic corner transistors, preventing premature gate dielectric breakdown [3–5] and minimizing the formation of stress-induced silicon defects which induce junction leakage current when propagated in subsequent thermal and implant processes. Numerous papers have reported the strain can change electron and hole mobilities in silicon by piezoresistive effects [6], such as silicon germanium for pMOSFET, silicon carbon for nMOSFET [7], stress memory technology (SMT) and stress liner of contact etch stop layer (CESL) [8–11]. However, STI stress effects caused by STI liner have been shown to diminish the nMOSFET performance degraded by STI compressive stress. In the study, we modify STI liner process to investigate STI stress effect on MOSFETs and 0.299 μm^2 cell size 6T-SRAM for 40 nm CMOS technology.

2. Experiment

The logic devices and 0.299 μm^2 cell size SRAM used in this work were fabricated on (1 0 0)/⟨1 1 0⟩ oriented p-type substrate with a 40 nm low-power CMOS technology. For a standard 40 nm CMOS process, STI trench is etched to a depth approximately 3000 Å. After trench formation, a SiON film is grown by pulse RF decoupled-plasma-nitridation (DPN) to replace pure oxide film by in situ steam generation (ISSG) process. The SiON film has two major processes: (1) around 15 Å base oxide was growth by rapid thermal oxidation (RTO); (2) decoupled-plasma-nitridation using nitrogen gas with 80 m Torr chamber pressure and 1800 W effective RF power. Subsequently, a high aspect ratio process using TEOS based sub-atmospheric chemical vapor deposition (SACVD) process at 540 °C is performed for void-free STI gap-fill [12]. After SACVD deposition, the 1050 °C densification anneal by furnace is used to reduce moisture in the film. Finally, the trench is planarized with chemical mechanical polishing (CMP). After STI process, N-well and P-well processes are applied. Then, ultra-thin gate dielectric is grown by pulse RF decoupled-plasma-nitridation (DPN) and uses in situ poly deposition with LPCVD. The poly

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patterning is using immersion lithography and accurate process controlled etching to control about 40 nm level poly length. An optimized halo and shallow source/drain extension (SDE) is designed for strict requirements to obtain lower leakage current and higher device performance. Finally, RTA with high temperature ramping is used for source and drain to form an ultra-shallow junction and higher activation of implant species.

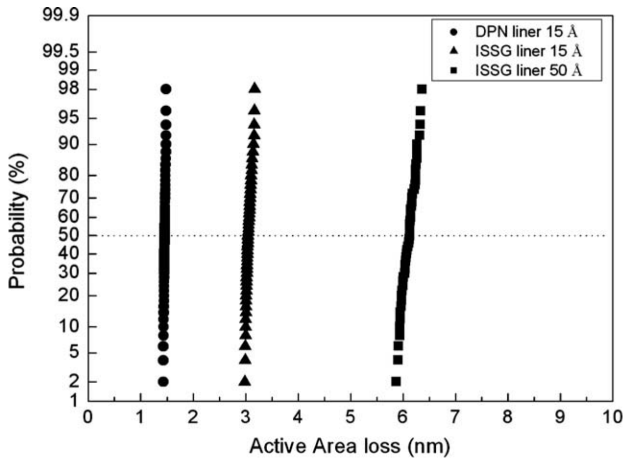

Fig. 1. The distribution of device active area loss for DPN SiON and ISSG pure oxide liners. The device active area loss is measured by critical-dimension difference between before-liner-deposition and after-liner-deposition for DPN and ISSG growths.

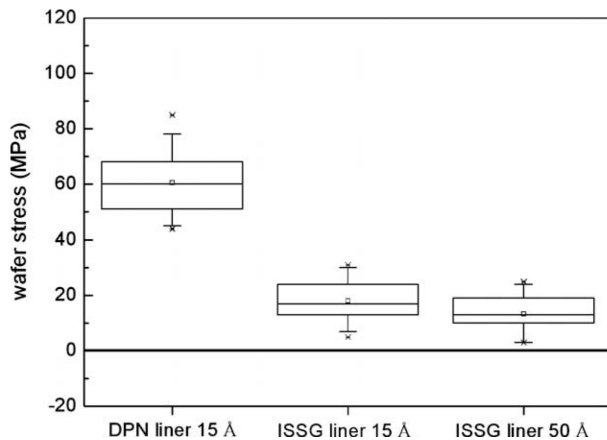

Fig. 2. Stress measurement for DPN SiON and ISSG pure oxide liners with different thickness. The measurement is performed after STI–CMP.

3. Results and discussion

In order to investigate active width loss caused by STI liner deposition for various pure oxide liners and SiON liner, we measure 126 nm STI-pitch of active area (72 nm) and STI gap-fill width (54 nm). We estimate critical-dimension difference between before-liner-deposition and after-liner-deposition in Fig. 1. As seen in Fig. 1, increasing the ISSG oxide liner thickness from 15 Å to 50 Å results in around 3 nm additional active width loss. Compared to pure oxide liner by ISSG growth of a similar thickness, SiON liner growth by DPN can reduce active width loss by around 1.5 nm. Therefore, SiON liner can suppress the oxygen diffusion towards the substrate and STI corner to avoid the oxidation induced active width loss.

For evaluating the film stress of STI gap-fill with different liners, we measure film stress from the wafer bow after STI–CMP since it is difficult to measure direct local stress in trench or active area. Fig. 2 shows post STI–CMP tensile stress for various STI liners. As shown in Fig. 2, the different pure oxide liners have minor influence on the stress. However, SiON liner has higher tensile stress than pure oxide liner while using the same gap-fill by SACVD. Therefore, STI stress can be adjusted by different STI liner formations.

From device point of view, we examine MOSFETs drive current (I_{on}, measured with gate (V_{GS}) and drain (V_{DS}) voltage equally at operation voltage (V_{DD} = 1.0 V)) with scaling active width since STI liner deposition results in active area loss as shown in Fig. 1. As shown in Fig. 3, I_{on} increases with scaling active width for various STI liners and thicker liner reduces I_{on} increase with scaling active width due to smaller active area. According to inverse narrow width effect (INWE), the I_{on} becomes higher and the threshold voltage (V_{th}) becomes lower for narrower transistor. Therefore, we use magnitude of I_{on} increase with active width shrink to evaluate INWE since narrow width devices are commonly used in system-on-chip (SOC) design currently. In order to evaluate STI stress effect, we examine junction leakage and length of diffusion (LOD) effect on MOSFETs since SiON liner has higher tensile stress than pure oxide liner as shown in Fig. 2. We evaluate LOD effect on I_{on} at various SA (active area dimension in the direction perpendicular to poly gate). Fig. 4 shows that nMOSFET I_{on} is increased with shrinkage in SA, but reverse trend in MOSFET due to tensile stress

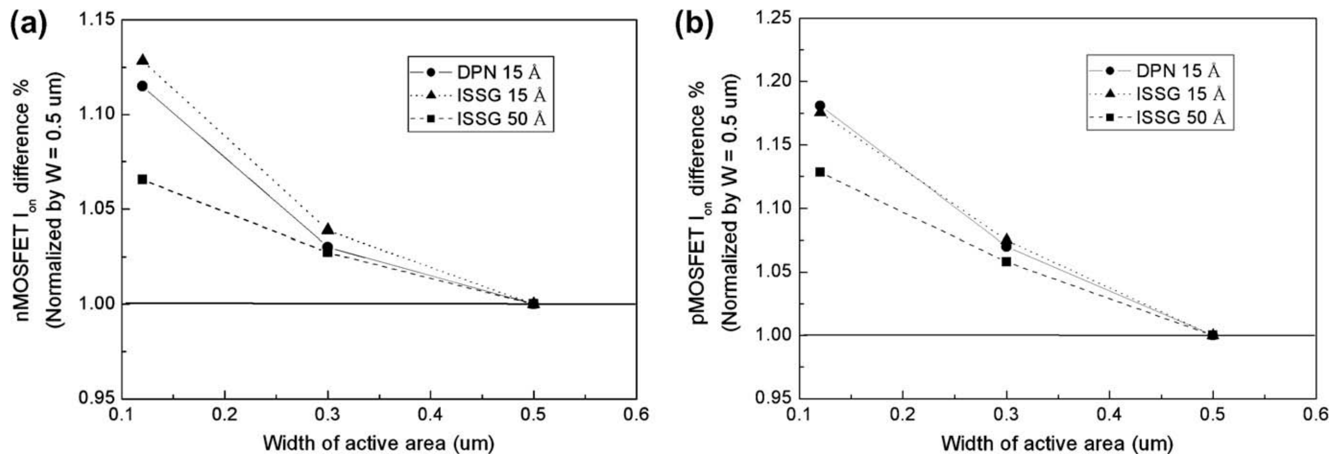

Fig. 3. Measured I_{on} on 40 nm poly length and normalized by large width (W = 0.5 μm) devices to observe narrow width effect with different DPN SiON and ISSG pure oxide liners for (a) nMOSFET and (b) pMOSFET.

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