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Facet engineering for SiGe/Si stressors in advanced CMOS technology

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ABSTRACT

A two-layer SiGe stressor was introduced for our CMOS technology containing a bottom layer with high Ge content to induce more stress to the channel and a top layer with lower Ge content for better nickel silicidation. However, even with the top lower Ge layer, defects were found after silicidation causing contact punch through. Since it is well known that the silicidation improves for Si, the SiGe top layer was replaced by a Si layer (Si-cap). Evaluation on 750 °C and 850 °C grown Si-cap was done. Different temperature grown Si-caps showed different growth behavior with morphology of the Si-cap grown at 850 °C completely different than that of the Si cap grown at 750 °C. There was a clear {3 1 1} facet formation for the higher temperature Si-cap resulting in a pinning effect to the spacer edge similar to that observed for the SiGe-cap. The faceted Si-cap improved silicidation and device parameters enabling the extension of this integration approach for SiGe/Si stressors to the more advanced technology nodes.

1. Introduction

A stressor to improve the pMOS performance had been introduced in our 90 nm CMOS technology initially as a single SiGe layer [1,2]. Unlike the first reported and nowadays widely used SiGe stressor integration [3], the SiGe was grown undoped prior to the transistor implants in order to enable optimal control of the dopant profile through implantation while keeping SiGe close to the gate [1,4]. In order to induce more stress into the channel, a higher Ge content in the SiGe stressor is required. However, the higher Ge content impacts on the nickel silicidation resulting in a high defectivity of the silicide. Thus, a two-layer SiGe stressor had been introduced in our 45 nm CMOS technology containing a layer with high Ge content to induce more stress to the channel and on top a layer with lower Ge content (cap layer) for better silicidation [5].

However, the silicide defectivity became more critical for more advanced technology nodes. A high number of defects were found after the silicidation of the SiGe top layer causing contact punch through. It was not feasible to achieve the required quality of the silicide using a SiGe-cap even with low Ge content. Since it is well known that the silicidation improves for Si [6], the SiGe top layer was replaced by a Si layer (Si-cap). In this paper we will present the challenges to introduce a Si cap layer for this integration approach in which the SiGe/Si stressor is grown prior to transistor implants. The morphology of the cap layer is critical for this integration scheme. Only a faceted Sicap layer that pins the cap to the nitride spacer edge enables healthy device parameters.

2. Experimental details

In this study, the SiGe S/D stressors were grown with commercially available epi reactor. The process flow involved a Si recess etch process using reactive-ion etching (RIE), followed by cleaning and subsequent selective epitaxial SiGe growth using reduced pressure chemical vapor deposition (RP-CVD) at about 700 °C with DCS, GeH4, and HCl. Initially, the Si cap that replaced the SiGe cap was grown at a widely used temperature of 750 °C using DCS and HCl. Later, a higher temperature (~850 °C) Si cap process was developed in order to enable facet formation. Cross-sectional transmission electron microscope (XTEM) was carried out to check the growth morphology of different caps grown on the SiGe. Finally, the device parameters were tested to analyze the electrical response of the samples with different stressors.

3. Results and discussion

SiGe-cap grown at ~700 °C shows a clear {3 1 1} facet resulting in a pinning effect at the spacer edge due to the lower growth rate on {3 1 1} (Fig. 1a). Si cap initially was grown at 750 °C to replace the SiGe-cap. However, the morphology of the Si-cap layer is changed compare to that of the SiGe-cap layer. The {3 1 1} Si-cap facet

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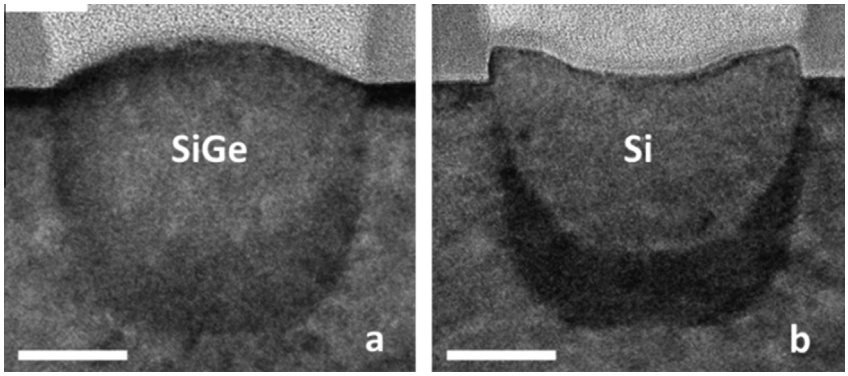

Fig. 1. TEM cross section right after deposition for (a) SiGe cap grown at 700 °C and (b) Si cap grown at 750 °C. Scale bar is 20 nm.

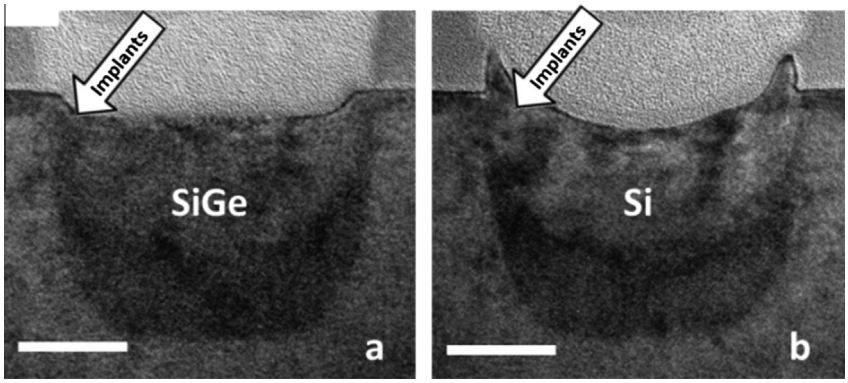

Fig. 2. TEM cross section before the extension/halo implantation for (a) SiGe cap and (b) Si cap grown at 750 °C. Scale bar is 20 nm.

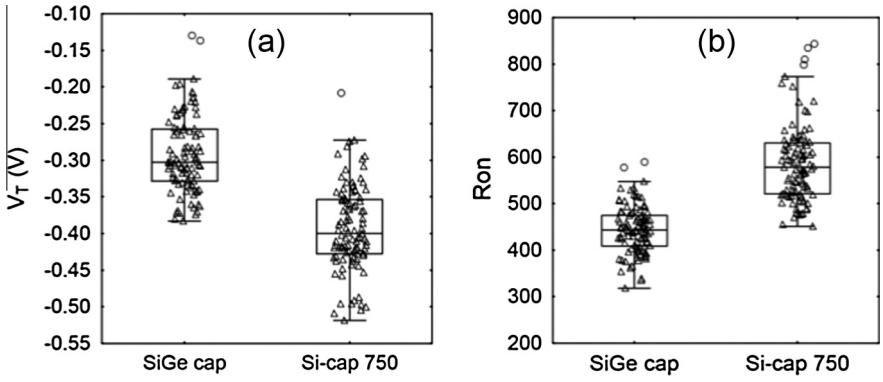

Fig. 3. (a) VT and (b) Ron for SiGe cap and Si cap grown at 750 °C.

did not form at low temperature and the Si growth was not pinned at the spacer edge (Fig. 1b).

Due to several cleaning steps between epitaxial deposition and implant, there is a certain loss of SiGe- or Si-cap. Fig. 2 shows the remaining morphology for SiGe- and Si-caps before the extension/halo implants. The loss of Si or SiGe is not uniform, and particularly differs at the spacer edge, influenced by their as-grown morphology.

Since critical transistor implants such as pMOS extension and halo implants are carried out later in the process flow, the SiGe source/drain shapes, especially the morphology near spacer edge, have direct impact on the device parameters. As shown in Fig. 2b, the 750 °C Si-cap has excess Si at spacer edge before implantation steps. Since the junction implant profile follows the surface of the remaining Si-cap, the junction profile is pulled up underneath the remaining Si-cap at the spacer edge causing a dopant gap and thus increased parasitic series resistance and artificially raised transistor threshold voltage (VT).

The impact of the Si-cap grown at 750 °C morphology on transistor threshold voltage (VT) is shown in Fig. 3a. There is a clear VT shift compared to that with SiGe-cap because the remaining Si at the spacer edge blocks the halo implants thus increasing VT. This VT shift could not easily be recovered by a higher extension dose or increased implant energy without the risk of lattice