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Design of an L1 band low noise single-chip GPS receiver in 0.18 μm CMOS technology

CHEN Ying-mei (✉), LI Zhi-qun, WANG Zhi-gong, JING Yong-kang, ZHANG Li

Institute of Radio Frequency and Electronic Integrated Circuits, Southeast University, Nanjing 210096, China

Abstract

This article presents an L1 band low noise integrated global positioning system (GPS) receiver chip using 0.18 μm CMOS technology. Dual-conversion with a low-IF architecture was used for this GPS receiver. The receiver is composed of low noise amplifier (LNA), down-conversion mixers, band pass filter, received signal strength indicator, variable gain amplifier, programmable gain amplifier, ADC, PLL frequency synthesizer and other key blocks. The receiver achieves a maximum gain of 105 dB and noise figure less than 6 dB. The variable gain amplifier (VGA) and programmable gain amplifier (PGA) provide gain control dynamic range over 50 dB. The receiver consumes less than 160 mW from a 1.8 V supply while occupying a 2.9 mm^2 chip area including the ESD I/O pads.

Keywords CMOS RF receiver, GPS, low IF, satellite communications, wireless communications

1 Introduction

Recently, wireless communications has been widely used in daily applications such cellular phones, PDAs or notebooks. The GPS is a satellite broadcast system providing absolute position, velocity and time information. Traditionally, GPS radio is implemented in bipolar technology. However, to satisfy the increasing demand for lower cost and higher levels of integration, CMOS implementation has become more popular.

The wireless system consists of a number of components, such as low noise amplifier, mixers, filters, power amplifiers, frequency synthesizers and base-band modems. In GPS applications, highly strict noise figure (NF) is required [1–3]. This is totally different from the case of Bluetooth, whose requirement for input sensitivity is at around −85 dBm, which is relatively easier to meet. The sensitivity target of this work is −110 dBm.

2 System model and problem formulation

Fig. 1 shows a block diagram of the GPS receiver. There are two options for receiver architecture. One is single conversion which is a simple architecture. The other is double conversion with a real filter requiring a two-stage IF, which enables the receiver to attenuate image signals. Every architecture has advantages and drawbacks, which together make them almost equally attractive. In this design, double conversion is used because of its superior 1/*f* noise reduction [4]. First, the low drop-out (LDO) regulator provides steady 1.8 V voltage supply from the 3.3 V external supply. Then, the radio part has an LNA in the front end, which requires low NF, low power, moderate gain, and a mixer to down-convert the 1 558 MH–1 578 MHz (L1 band) RF signal. Two PLL synthesizers generate local frequency. The first mixer down-converts the LNA output to the first IF signal at approximately 180 MHz. After filtering the out-of-band spectrum and amplifying the first IF signal, the second mixer down-converts the signal again to the second IF at approximately 46 MHz. The received signal strength indication (RSSI) provides a DC analog level to the VGA. The VGA or PGA is used to amplify the baseband signal further to handle a wide input signal range. The ADC converts the analog signal to binary digital data coded as sign (SIGN) and magnitude (MAG) bits to a digital correlated chip. In this GPS receiver, the serial peripheral interface (SPI) can fulfill VGA and PGA loop switch, LO frequency control, PLL lock state indicate and so forth.

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Corresponding author: CHEN Ying-mei, E-mail: njcym@seu.edu.cn
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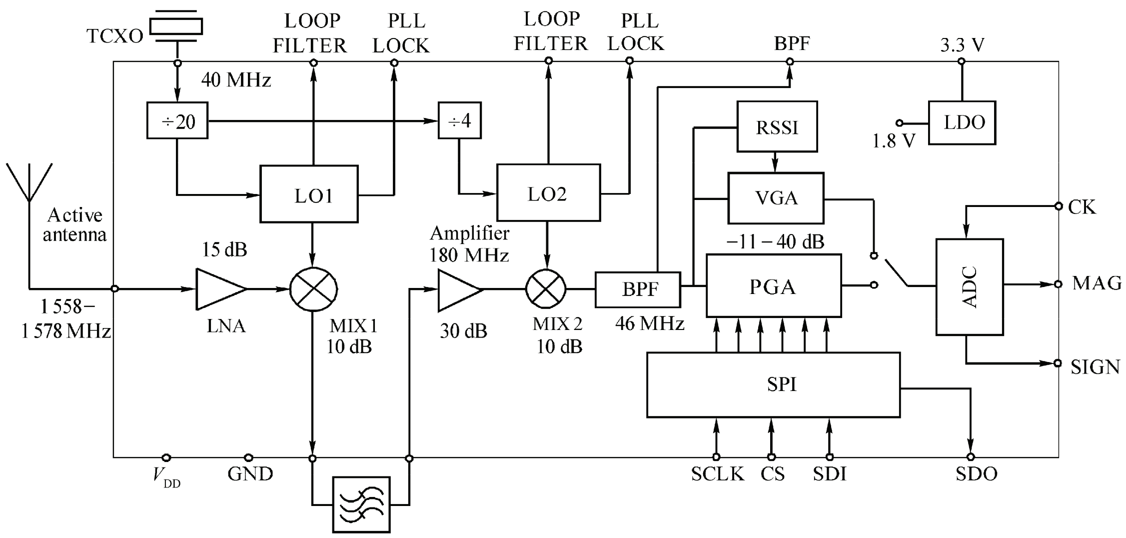

Fig. 1 Block diagram of the GPS receiver

3 Circuit design

3.1 RF section

The LNA design aims at minimizing the noise figure, providing enough gain with sufficient linearity and providing a stable 50 Ω input impedance to achieve good input matching [5]. The LNA uses a single-to-differential architecture because the first mixer should be a double-balanced mixer to minimize the LO feed-through that will cause an unacceptably large DC offset at the second mixer output. In Fig. 2, the input stage M_1 is an inductively degenerated common source stage and the input impedance can be expressed as [6]

$$Z_{in} = \frac{1}{j\omega C_{GS}} + j\omega(L_G + L_S) + \omega_T L_S \quad (1)$$

where ω_T is the transient frequency of the transistor.

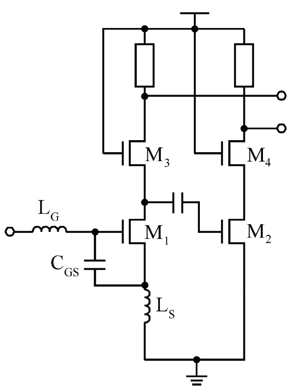

Fig. 2 Schematic of LNA

The gain of the LNA was specified as 15 dB, while the requirements for both the noise figure and IIP3 are quite moderate, with values of 1.5 dB and −10 dBm, respectively.

Fig. 3 shows the schematic of the RF mixer. A conventional Gilbert-type mixer, with a source-grounded input stage and a current bleeding technique at the load, is used to achieve high gain and low-voltage operation. The RF section acquires a total gain of 25 dB, cascaded noise figure of less than 2 dB and IIP3 of −18 dBm.

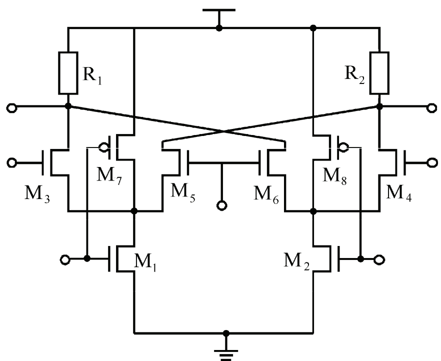

Fig. 3 Schematic of RF mixer

3.2 IF section

The operating frequency of the band pass filter (BPF) is 46 MHz. The schematic of the BPF is shown in Fig. 4. It consists of four transconductors (g_{1d} or g_{2d}) blocks or transconductors, which are linearly differential pairs and capacitors. Transconductors have low gain but a large input range extended by means of linearization techniques such as local feedback and cross-coupling. They can provide possibly high filter frequencies with reasonable quality factors [7]. To cancel out the even-order harmonics, a differential version is preferred. The transform function, center frequency and