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Passive mixer with OPA filter for DVB-H front-end in 65 nm digital CMOS technology

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ABSTRACT

This paper presents a passive mixer combined with a 1st-order active low-pass filter implemented in a purely digital low-power 65 nm CMOS technology. The filter consists of a four-stage operational amplifier with two feed-forward paths for a 3 dB corner frequency of 4 MHz. The mixer offers a very low flicker noise corner frequency of 80 Hz for DVB-H application. A fabricated test chip with integrated clock regeneration circuit offers even for a very small clock input signal amplitude a maximum gain of 26 dB. The combination offers an IIP_3 of -5 dBm while the mixer consumes 12.27 mA and the filter 4.42 mA from a 1.25 V supply.

1. Introduction

Digital Video Broadcast for Handheld (DVB-H) is a mobile television standard based on Digital Video Broadcast for Terrestrial (DVB-T). It is specifically designed for mobile devices like mobile phones. Due to the fully backward compatibility to DVB-T, the already existing infrastructure can be used and a large geographical area can be reached with the signal. DVB-H is a point-to-multipoint connection in contrast to UMTS which is a point-to-point connection. The multipoint approach offers the advantage of high data throughput to multiple consumers at the same time while only occupying a small frequency spectrum for transmission [1].

For mobile receiving devices, low power consumption is a very important aspect. Furthermore such systems need to be fully integrated in one technology. Integration of the entire receiver in one technology reduced fabrication costs as only one set of masks has to be fabricated and it also reduces parasitic elements which arise when multiple integrated circuits are connected together. These are inductances from bond wires and capacitances from bonding pads. Fig. 1 shows the block diagram of a direct I/Q conversion receiver [2] which is the preferred implementation for such fully integrated receiver systems. It consists of an antenna and usually some sort of band-pass filter. In the diagram a surface acoustic wave (SAW) filter is indicated because such filters have superior performance at high frequencies compared to active filters. As close to the antenna as possible a low noise amplifier (LNA) is placed to amplify the signal for further processing in the receiver chain. After the first amplification two separate signal chains, the inphase (I) and quadrature (Q) chains are placed. With this technique digital image rejection is achieved. After down-conversion of the signal into the baseband, a low-pass filter limits the bandwidth of the received signal to 4 MHz. This 4 MHz is the channel bandwidth of the different DVB-H channels. After the filtering, an analog to digital converter (ADC) converts the signal into the digital domain where the baseband processing can be performed in a digital signal processor (DSP) or microprocessor.

2. Circuit overview

We implemented a passive mixer in combination with a first order low-pass filter for one of the direct conversion receivers. Fig. 2 shows the block diagram of a test chip with the passive mixer in combination with the filter. The test chip has an additional circuit block, the clock regeneration circuit, which is needed for characterization by measurement. This clock regeneration circuit is used for reshaping the applied differential clock to a full logic swing. For operation of the passive mixer it relies on the g_m-cell. This g_m-cell converts the applied input voltage signal to a current signal for the passive mixer core itself.

A passive mixer is used to minimize the flicker noise in the receiver system due to the small bandwidth of the channel and

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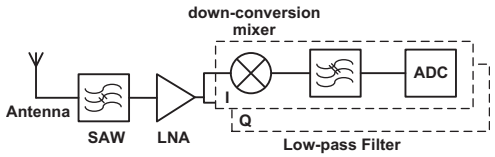

Fig. 1. Direct I/Q conversion receiver.

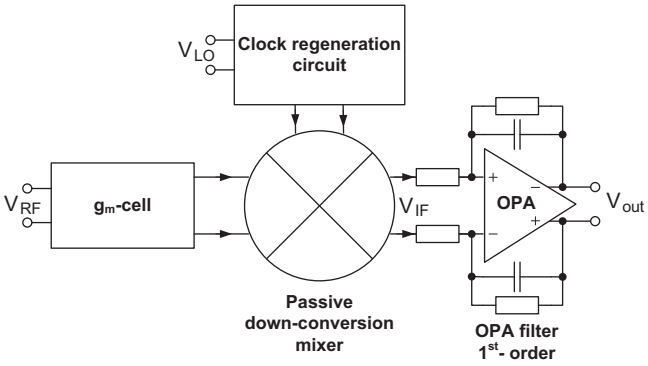

Fig. 2. Block diagram of the implemented test chip.

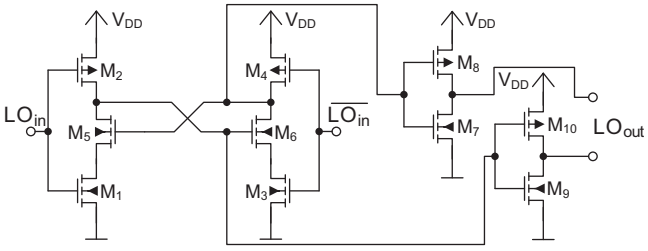

Fig. 3. Clock regeneration circuit.

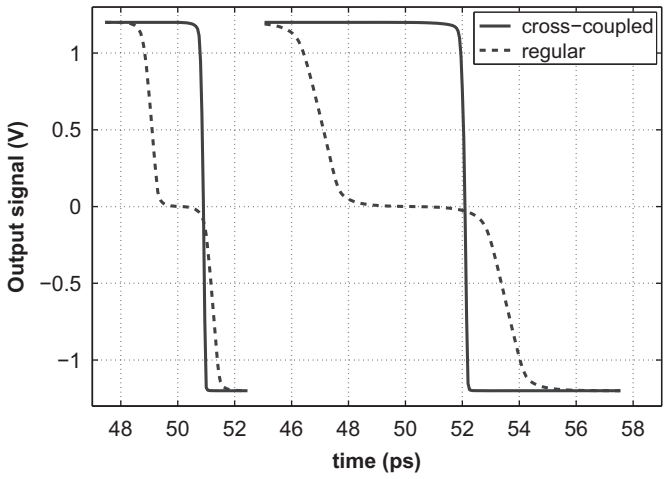

Fig. 4. Transient simulations of regular inverter and cross-coupled inverter output.

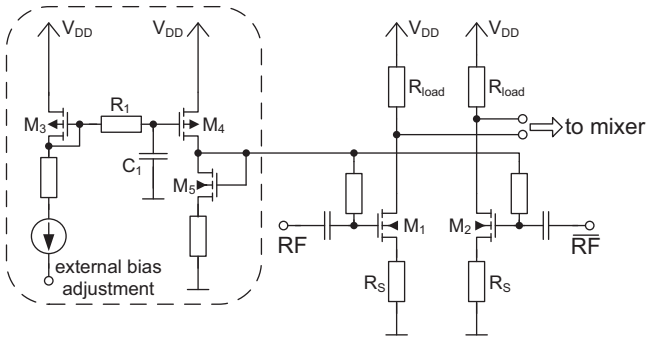

Fig. 5. g_m-cell for voltage signal to current signal conversion.

the high flicker noise in the used 65 nm digital CMOS technology [3]. The 1st-order low-pass filter is implemented as an operational amplifier (OPA) filter with RC feedback. The amplifier is a fully differential four-stage operational amplifier with two feed-forward paths. A class AB output stage is implemented and the entire OPA is compensated with a nested Miller compensation network. The OPA itself is published in [4]. It offers a gain-bandwidth product of 1 GHz with a phase margin of 60° measured at a load capacitance of 4 pF. The OPA has a DC gain of 68 dB. It consumes 9.6 mA from a supply voltage of 1.2 V and has a power supply rejection ratio of 77 dB. The circuit has an input referred noise voltage of 1.73 nV/$\sqrt{}$Hz at a frequency of 1 MHz.

3. Clock regeneration circuit

The clock regeneration circuit is needed to have a full swing digital signal for the switching transistors in the passive mixer circuit. With a better switching characteristic, also the performance parameters of the entire circuit increases. To avoid the need for a very large differential clock signal at the input, the signal is rectified directly on chip with the circuit show in Fig. 3. A differential signal LO_{in} is applied at the input to the two cross-coupled inverters which consists of the transistors M_1–M_6. The transistors M_5 and M_6 introduce an additional feedback to the inverters for a higher gain in the inverter stage. This circuit configuration offers the advantage, that even for small input amplitudes a full swing digital output signal will be generated.

Fig. 4 shows the results of a transient simulation in Cadence to confirm the better behavior at the output LO_{out} of the clock regeneration circuit. The solid line is the transient response of the clock regeneration circuit with cross-coupled transistors M_5 and M_6. The dotted line shows the behavior of the circuit if only regular inverters would be used. On the left part of the figure the differential signal at the output of the clock regeneration circuit is shown for a sinusoidal input signal with amplitude of 1.2 V. It shows a short plateau of approximately 2 ps in the middle of the transition for regular inverters. The solid line shows the output transition with the cross-coupling in the inverters. This transition is much steeper compared to a simple inverter used for clock regeneration. The right side of the figure shows again the same signals but for an input signal with an amplitude of 0.4 V. Here it is even more clearly visible that a simple inverter would have a rather long plateau in the middle of the transition. For the cross-coupled structure, the steep transition is about the same for the smaller input amplitude as for the larger input signal. The improvement with the cross-coupled inverters in the clock regeneration circuit provides a constant overall circuit performance for a large clock amplitude range.

4. Passive mixer circuit

The passive mixer relies on the g_m-cell to provide a current signal for down-conversion. The schematic of this circuit part is shown in Fig. 5. A biasing circuit provides a DC-bias for the two input transistors M_1 and M_2. The bias condition can be externally adjusted with an applied DC current through transistor M_3.