Characterization of logic circuit techniques and optimization for high-leakage CMOS technologies ☆

Phillip Chin[a],[*],[1], Charles A. Zukowski[a], George D. Gristede[b], Stephen V. Kosonocky[b]

[a]*Department of Electrical Engineering, Columbia University, 500 West 120th Street, NY 10027, USA*
[b]*IBM T.J. Watson Research Center, 1101 Kitchawan Road, P.O. Box 218, Yorktown Heights, NY 10598, USA*

Abstract

Channel subthreshold and gate leakage currents are predicted by many to become much more significant in advanced CMOS technologies and are expected to have a substantial impact on logic circuit design strategies. To reduce static power, techniques such as the use of monotonic logic and management of various evaluation and idle modes within logic stages may become important options in circuit optimization. In this paper, we present a general, multilevel model for logic blocks consisting of logic gates that include a wide range of options for static power reduction, in both the domains of topology and timing. Existing circuit techniques are classified within this framework and experiments are presented showing how aspects of performance might vary across this range in a hypothetical technology. The framework also allows exploration of optimal mixing of techniques.
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1. Introduction

Power dissipation has become an extremely important constraint in modern micro-processor design as CMOS technologies continue to advance. This power issue is driven by concerns about circuit reliability, packaging costs, and the proliferation of mobile devices dependent on battery life. Historically, power dissipation in CMOS circuits has primarily been the result of the charging and discharging of load capacitances, referred to as dynamic power dissipation. However, as we begin to enter the realm of sub-100 nm technology, static power consumption is expected to become much more important. The maximum number of transistors on chips will increase dramatically. Supply voltages will continue to scale to reduce dynamic power, and threshold voltages will decrease to maintain transistor switching speeds. This will result in an increase in subthreshold current conduction. Also, decreasing gate oxide thicknesses will reach the 1.2–1.5 nm regime, where direct tunneling current will become significant. This combination of subthreshold and gate leakage will have a substantial impact on idle-state leakage currents, and greatly increase the standby leakage power of highly integrated circuits [1]. The International Technology Roadmap for Semiconductors predicts an exponential increase in leakage current over time as scaling continues [2]. These scaling issues will require consideration of both static and dynamic power in future circuit designs [3–6].

The potential impact of subthreshold and gate leakage currents must be well understood, either to deal with this growing problem or to evaluate the technology tradeoffs involved in avoiding it. A number of specific circuit techniques have been proposed that might help deal with this issue. Previous work in leakage resistant circuit topologies can be placed into two categories, critical path and non-critical path techniques. Non-critical path techniques that reduce leakage current at the expense of increased circuit delay include transistor sizing, transistor stacking [7–9], higher threshold voltages [10], lower supply voltage, and thicker oxides: collectively, these techniques have been referred to as statically selected slow transistors (SSSTs). In critical paths, idle portions of circuits with fast, leaky devices are deactivated with techniques such as body biasing [11], input vector control [12], and sleep transistors [10]: these techniques have been collectively referred to as dynamically deactivated fast transistors (DDFTs) [13]. However, the entire spectrum of circuit options has not been fully explored yet, and the potential for mixing techniques has received little attention. Furthermore, studies have often been limited to technologies that are not too different than current ones, and have focused primarily on subthreshold conduction alone.

In this paper, we present a general model (introduced in [14]) in Section 2 that includes likely topology and timing approaches for restoring logic circuit design. A framework is introduced to allow optimal mixing of circuit techniques. A key contribution is the inclusion of monotonic logic in its basic form, based on observations that it has some key advantages for high leakage technologies. Section 3 contains examples of how some specific circuit techniques can be viewed as a special instance of the model. Some simple experiments are presented in Section 4, showing how our design framework can be used to optimize a logic block using partial monotonicity. Adjustment of transistor type and size is added to the results presented in [14].