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Microelectronics Journal 33 (2002) 1059–1069

Microelectronics  
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# A novel topology for grounded-to-floating resistor conversion in CMOS technology

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Received 8 February 2002; revised 4 July 2002; accepted 23 August 2002

## Abstract

A new circuit topology to convert grounded resistors to an equivalent floating resistor is presented and discussed. The value of the resulting floating resistor equals the sum of the two grounded resistors. The new topology can be used to convert either passive, active grounded resistors or active grounded conductances. The new topology is used in the design of a current controlled very high value floating resistor in the range of  $G\Omega$ . This was achieved by utilising the output conductance of two matched transistors operating in the subthreshold region and biased using a 500 nA current. The practicality of the new topology is demonstrated through the design of a very low frequency bandpass filter for artificial insect vision and pacemaker applications. Simulations results using Level 49 model parameters in HSPICE show an introduced total harmonic distortion of less than 0.25% for a 1  $V_{pp}$  input signal in a 3.3 V 0.25  $\mu\text{m}$  CMOS technology. Statistical modelling of the new topology is also presented and discussed.

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*Keywords:* Active floating resistors; Very low frequency BP filter; Low frequency differentiator; Artificial insect vision; Pacemaker

## 1. Introduction

Resistors and transconductors have a very important role in a wide variety of applications such as signal processing and neural networks, which rely heavily on the design of analog VLSI circuits. Due to the large area penalty of using passive resistors, wide spread, lack of accuracy and programmability [1,2], a large number of implementations of active resistors and transconductors using MOS transistors have been discussed in literature [3–11]. Some of these techniques exploit the MOS transistor characteristic in the triode [2,12,13], saturation regions [2] and few exploit the subthreshold region of operation [14,15]. The new topology can be used to obtain low-power high-value floating resistors with high linearity and wide dynamic range.

Section 2 of this paper presents and discusses the theoretical background and the implementation of the new circuit topology in standard CMOS technologies. Section 3 demonstrates the use of the new topology in converting voltage controlled grounded resistors to a

voltage controlled floating resistor. Section 4 discusses the use of the new topology in the design of a current controlled very high value floating (VHVF) resistor. Section 5 presents and discusses statistical modelling of the new topology using passive resistors. Section 6 presents a practical example of using the new current controlled very high value resistor in the design of a current controlled differentiator circuit, which has practical use in artificial insect vision [16] and pacemaker applications.

In the following analysis it is assumed that the source and the back gate for the corresponding n and p type MOS transistors are connected together, unless mentioned otherwise.

## 2. A new circuit topology

### 2.1. Theoretical analysis

The new topology is based on two-diode connected matched transistors operating in the saturation region [17] as shown in Fig. 1.  $V_x$  and  $V_y$  are the floating resistor terminal voltages, and  $I_{in} = I_{out}$  is the current passing through

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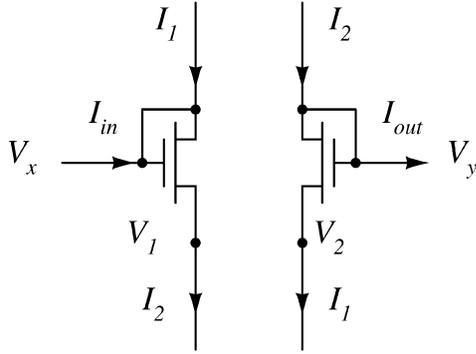


Fig. 1. The basic MOS transistor cell.

the terminals. The current equation for the transistors in Fig. 1 can be written as

$$I_1 = \frac{K}{2}(V_y - V_2 - V_{th})^2, \quad (1)$$

$$I_2 = \frac{K}{2}(V_x - V_1 - V_{th})^2, \quad (2)$$

where  $K$  is defined as  $\mu_o C_{ox}(W/L)$ ;  $\mu_o$ , the carrier mobility;  $C_{ox}$ , the oxide capacitance per unit area;  $V_{th}$ , the MOS transistor threshold voltage and  $W/L$  is the width to length ratio of the transistor. The current passing through the circuit topology can be written as

$$I_{in} = I_{out} = I_2 - I_1. \quad (3)$$

Substituting Eqs. (1) and (2) into Eq. (3), and simplifying the results,  $I_{out}$  can be written as

$$I_{out} = \frac{K}{2}[(V_x - V_y) - (V_1 - V_2)][(V_x + V_y) - (V_1 + V_2) - 2V_{th}]. \quad (4)$$

The equivalent resistance,  $R_{eqv}$ , is defined as

$$R_{eqv} = \frac{V_x - V_y}{I_{in}} = \frac{V_x - V_y}{I_{out}}. \quad (5)$$

In order to achieve a circuit topology independent of the MOS transistor threshold voltage, let

$$V_1 = V_x - V_{th} + f(V_x), \quad (6)$$

$$V_2 = V_y - V_{th} + f(V_y). \quad (7)$$

The sum and the difference of  $V_1$  and  $V_2$  can be written as

$$V_1 + V_2 = V_x + V_y - 2V_{th} + f(V_x) + f(V_y), \quad (8)$$

$$V_1 - V_2 = V_x - V_y + f(V_x) - f(V_y). \quad (9)$$

By substituting Eqs. (8) and (9) in Eq. (4),  $I_{out}$  can be written as

$$I_{out} = \frac{K}{2}(f(V_x)^2 - f(V_y)^2). \quad (10)$$

Eq. (10) shows that the current passing through the topology is independent of the MOS transistor threshold voltage, a square function of  $V_x$  and  $V_y$  and is proportional to  $K$ .

## 2.2. Topology implementation

A possible implementation of Eqs. (6) and (7), is shown in Fig. 2. In this topology the current passing through  $mn_1$  is mirrored by  $mn_2$  and feeds back to the  $V_y$  terminal of  $mn_3$  using  $mp_1$ . In a similar way, the current passing through  $mn_3$  is mirrored by  $mn_4$  and feeds back to the  $V_x$  terminal of  $mn_1$  using  $mp_3$ . The relation between  $V_x$  and  $V_1$ , while assuming a passive resistor connected between  $V_1$  and ground, can be written as

$$V_1 = R(2I_2) = KR(V_x - V_1 - V_{th})^2, \quad (11)$$

where  $R$  is the resistor value. Solving Eq. (11) for  $V_1$  gives two solutions, the feasible one is

$$V_1 = V_x - V_{th} + \frac{1 - \sqrt{1 + 2KR(V_x - V_{th})}}{2KR}. \quad (12)$$

A similar expression for  $V_2$  can be written as

$$V_2 = V_y - V_{th} + \frac{1 - \sqrt{1 + 2KR(V_y - V_{th})}}{2KR}. \quad (13)$$

Comparing Eqs. (12) and (13) with Eqs. (6) and (7), respectively,  $f(V_x)$  and  $f(V_y)$  can be written as

$$f(V_x) = \frac{1 - \sqrt{X}}{2KR}, \quad (14)$$

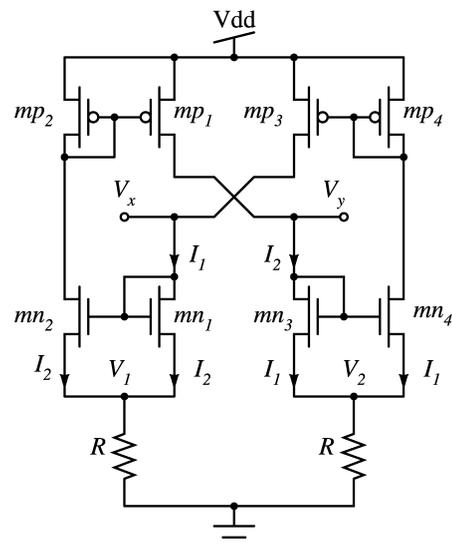
$$f(V_y) = \frac{1 - \sqrt{Y}}{2KR}, \quad (15)$$

where

$$X = 1 + 2KR(V_x - V_{th}) \text{ and } Y = 1 + 2KR(V_y - V_{th}).$$

Substituting the values of  $f(V_x)$  and  $f(V_y)$  from Eqs. (14) and (15) in Eq. (10),  $I_{out}$  can be written as

$$I_{out} = \frac{1}{8KR^2}[(1 - \sqrt{X})^2 - (1 - \sqrt{Y})^2]. \quad (16)$$

Fig. 2. The new topology with two passive resistor connected at  $V_1$  and  $V_2$  and ground.

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