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Investigation of iridium as a gate electrode for deep sub-micron CMOS technology

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Abstract

The physical and electrical properties of an $Ir/SiO_2/Si$ stack were evaluated for advanced gate electrode application. The thermal stability of the stack was studied on MOS capacitors annealed at temperatures between 500 and 1000 °C in N_2 ambient for 30 s followed by forming gas anneal (FGA) at 420 °C for 20 min. The work function of iridium, found to be 4.9 eV, is stable up to 900 °C, making it a good candidate as PMOS electrode. In addition, no evidence was found for any chemical reaction at the interface between Ir and SiO_2.

Keywords: Metal gate; Work function; Iridium

1. Introduction

Scaling of CMOS devices requires reduction of the capacitance equivalent thickness. The contribution of poly-depletion inherent to currently used poly-Si gates becomes more significant for aggressively scaled dielectric thickness. A realistic solution for the 45-nm CMOS technology node involves the introduction of metal gates that do not exhibit poly-depletion [1]. Another advantage of metal gates is the elimination of boron penetration into the channel. To replace n^+ and p^+ poly-Si gates, appropriate metals must be selected such that the work function can be selectively tuned for optimal operation of p- and n-type transistors requiring 5.17 and 4.05 eV, respectively [2]. Several metallic systems have already been proposed as potential candidates, such as Mo and $TaSi_xN_y$ for p-MOS and n-MOS, respectively [3,4]. However, some practical problems remain unsolved such as the stability of the work function during device processing and passivation of the interface states.

In this paper, we investigate the properties of Ir as a metal gate for p-type transistors. Using capacitance–voltage (CV) measurements on MOS capacitors, we study the influence of the annealing temperature on the Ir work function. Using X-ray diffraction (XRD) analysis, the $Ir/SiO_2/Si$ stack morphology is investigated and the annealing conditions that minimize the effective oxide charge are optimised.

2. Experimental

MOS capacitors were fabricated on (100) oriented

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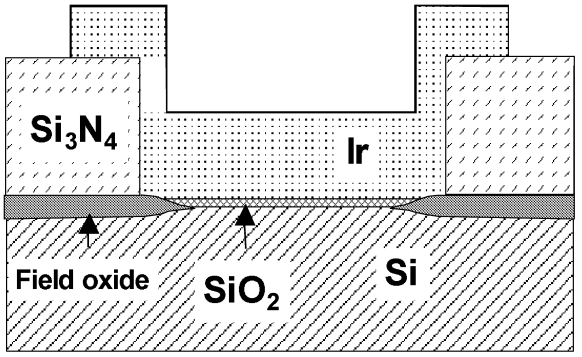

Fig. 1. Scheme of the MOS capacitor.

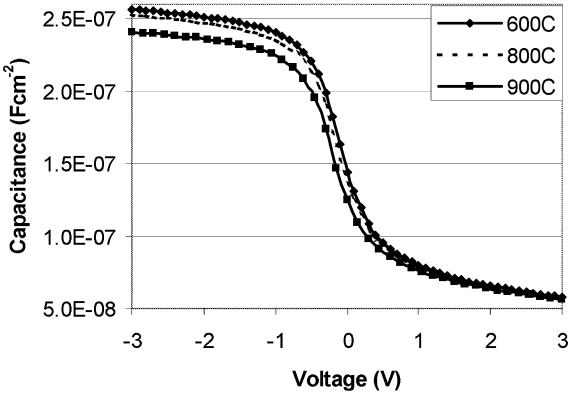

Fig. 2. High frequency CV characteristics on the $Ir/SiO_2/Si$ capacitors with 15-nm dielectric thickness annealed in N_2 to 600, 800 and 900 °C followed by FGA at 420 °C for 20 min. The flat band voltage shift corresponds to the change in effective oxide charges.

p-type silicon wafers. Ir films, 100 nm thick were sputtered at 150 °C on thermally grown SiO_2. The thickness of the dielectric varied between 6.5 and 25 nm. The iridium gate electrodes were made with an Si_3N_4 based gate last process using a hardmask based dry etch. The areas of the capacitors were defined by a poly buffered LOCOS isolation located under the Si_3N_4 layer. The capacitor scheme is presented in Fig. 1. All samples were annealed in N_2 ambient for 30 s at temperatures varying between 500 and 1000 °C. To passivate the interface states, samples were also annealed in forming gas (FGA) at 420 °C for 20 min.

To examine the thermal stability of the $Ir/SiO_2/Si$ stack, high-frequency capacitance–voltage measurements (HF-CV) were carried out on the MOS capacitors with an area of 10^{-4} cm^2 at each of the selected annealing temperatures using an HP 4284.

Phase formation and change in the crystallinity of the Ir layer upon annealing were determined by XRD. The chemical stability of the stack was investigated for changes in the Ir/SiO_2 interface by TEM inspection. The sheet resistance was examined by four point probe measurements on a SSM240 system.

3. Results and discussion

The HF-CV characteristics of $Ir/SiO_2/Si$ MOS capacitors are shown in Fig. 2.

A negative shift in flat band voltage (V_{FB}) was observed following annealing to 900 °C. According to the formula:

$$V_{FB} = \phi_{MS} - \frac{Q_i}{(\varepsilon_{ox}\varepsilon_0)d_{ox}}$$

where ϕ_{MS} is the Fermi level difference between the gate and the substrate, Q_i is the density of fixed oxide charges, ε_{ox} is the dielectric constant, ε_0 is the permittivity of free space and d_{ox} is oxide thickness; the V_{FB} shift indicates a decrease in work function of Ir or/and an increase in positive charges in the oxide. In order to distinguish between these two effects, the work function and effective oxide charges were extracted from CV measurements. By plotting V_{FB} versus equivalent oxide thickness (EOT) for different annealing temperatures, we found that the work function of Ir is 4.9 eV and that it is stable up to 900 °C as shown in Fig. 3. The slope of this linear plot indicates that effective oxide charges increase from 7×10^{10} to 3×10^{11} cm^{-2} following annealing to 600 and 900 °C, respectively. Thus, the V_{FB} shift is attributed to a change in charge content within the dielectric rather than a work function change.

HF-CV characteristics only show a change in EOT following annealing to 900 °C. Nevertheless TEM analysis performed on a sample annealed to 900 °C for 30 s, does not suggest chemical reaction at the interface between Ir and SiO_2 as shown in Fig. 4. In Fig. 5, XRD patterns of Ir films deposited on SiO_2 annealed at various temperatures in N_2 for 30 s are