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Highly sensitive Hall sensor in CMOS technology

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Abstract

We present a highly sensitive Hall device fabricated in a standard CMOS technology and combined with integrated flux concentrators acting as magnetic amplifiers. The active area of the Hall plate is in a buried n-well with a shape optimized by removing the parts less sensitive to the magnetic field. The effect of the shape of the concentrators is studied. This results in the design of elliptical shape integrated concentrators for the optimization of the sensitivity, and of the measurement range, as well as for the decrease of the overall chip size. The CMOS sensor combined with the optimized concentrators has a sensitivity of 2.1 V/T with a 4 V bias, the lowest detectable field is 0.2 μT in a frequency range of 10^{-3}–10 Hz and the linearity is better than 1% in a ±16 mT measurement range.

Keywords: Hall sensor; CMOS compatible; Ferromagnetic flux concentrators; High sensitivity; Low noise

1. Introduction

Currently, magnetic flux concentrators are widely used to increase the detectivity of magnetic sensors [1,2], but they are all discrete components assembled ‘‘off chip’’. However, it is shown in Ref. [3] that the combination of Hall devices with integrated flux concentrators allows to achieve high sensitivity. The first sensor designed to be used with integrated concentrators was the cylindrical Hall device [4] sensitive to the cylindrical field found under the air gap between two concentrators (Fig. 1). This sensor being designed in an n-substrate technology suffers from its incompatibility with modern CMOS processes where p-substrate are commonly used; this prevents the realization of the sensor and the electronics for signal processing on the same chip. In this paper, we present a new and highly sensitive Hall device designed in the n-well of a standard CMOS technology, with a shape compatible with the use of integrated flux concentrators. We also present the optimization of the shape of the flux concentrators that allows us to achieve higher sensitivity, smaller size and optimized measurement range.

2. CMOS highly sensitive Hall sensor

The development of a new technology for the production of integrated flux concentrators, realized directly on the wafer with a low-cost process using standard photolithography steps, has led to the realization of the cylindrical Hall device. The place required for the flux concentrators is larger than the size of the Hall sensor. Free space is thus available for the integration of signal processing electronics on the sensor chip. To do so, we have developed a new and highly sensitive Hall device compatible with modern CMOS technologies.

2.1. Reminder: cylindrical Hall device

The cylindrical Hall device (Fig. 1) has five contacts; the bias current flows from the central contact (Ic) to the two external ones (I2′, I2″) and the Hall voltage is measured between the two sense contacts (S1 and S2). It has low offset, low noise, and is especially suitable for applications where a low-power consumption is required, but it is not CMOS compatible.

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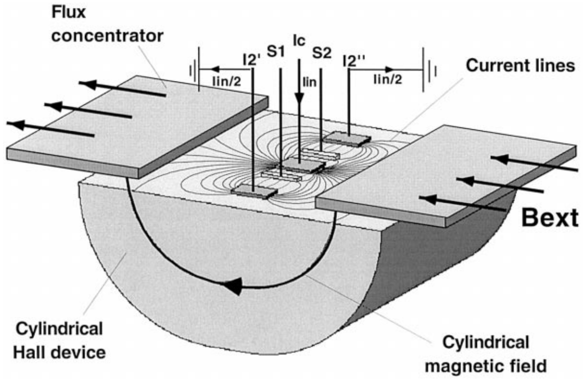

Fig. 1. Cylindrical Hall device sensitive to the cylindrical field under the air gap between two flux concentrators.

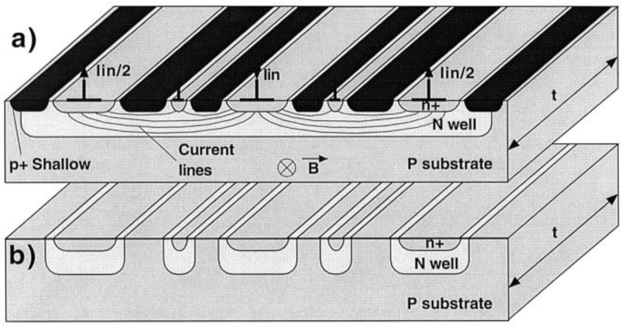

Fig. 3. Central part of two CMOS versions of the cylindrical Hall device. In a preliminary version (a), the sensitivity is decreased by the current that flows in a degenerate very thin Hall sensor. After optimization (b), this current is avoided by the p-substrate zones.

2.2. New CMOS hall device

The direct way to design a CMOS sensor based on the cylindrical Hall device would be to copy the design of the cylindrical Hall device and to define the active area with the n-well. The result of such a design is shown in Fig. 2. This device shows a contact distribution similar to that of the cylindrical Hall device. Since it is a planar device, the sensitivity to a cylindrical field is lost but it is still sensitive to the part of the field leaving the concentrators perpendicularly to the wafer plane. However, as explained below, the design of this sensor is not optimal.

The sensor shown in Fig. 2 can be considered as a combination of three Hall devices connected in parallel: the left side, the right side, and the central part constituted by the n-well portion below the contacts. A cut view of the central part through the cut plane shown in Fig. 2 is shown in Fig. 3a. This part of the sensor is a degenerate very narrow and very thick five-terminal parallel field Hall sensor with a very low sensitivity. A device constituted of the central part only has been realized and tested. A current related sensitivity of only 0.3 V/T has been measured. The left side and the right side of the sensor are devices close to conventional five-terminal parallel field Hall sensors. The Hall voltage at the output of the sensor shown in Fig. 2 will be an average value of the Hall voltages obtained for each of the three parts in parallel. As the central part produces a very low Hall voltage, the sensitivity of the global sensor is decreased. As a part of the current that flows directly between the contacts in the central region (see Fig. 3a), the power consumption is high.

But the direct conduction between contacts in the central part can be avoided by designing the n-well in such a way as to have p-substrate zones between the contacts (Fig. 3b). In this case, the Hall sensor is only constituted by the left side and the right side devices connected in parallel; the central part provides the connections of the sensor (see Fig. 4). This sensor can be viewed as a combination of two five-terminal parallel field Hall devices connected in parallel. In the way they are connected, the global sensor is sensitive to the magnetic field difference between the two sides. When this sensor is combined with flux concentrators, the magnetic fields seen by each side are of opposite sign. This gives the maximum magnetic field difference, and thus, the maximum output voltage. Compared to the CMOS Hall sensor of Fig. 2 with the central zone as shown in Fig. 3a, the current-related sensitivity of the optimized sensor shown in Fig. 4 is doubled.

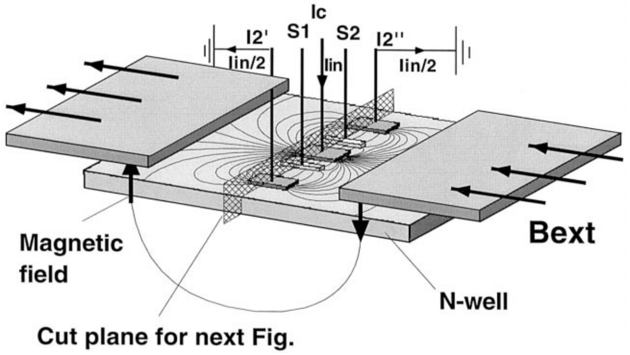

Fig. 2. Transposition of the cylindrical Hall device in a CMOS design. The n+ contacts position is copied and the active area is defined in an n-well.

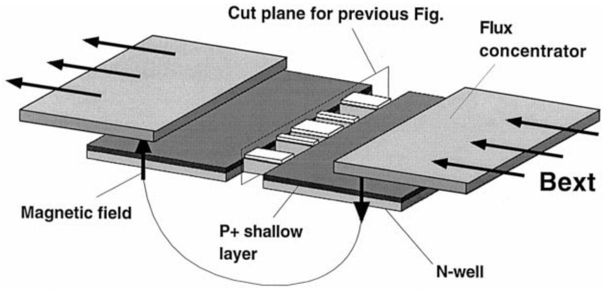

Fig. 4. Highly sensitive CMOS Hall sensor integrated in an n-well. A p+ shallow layer prevents surface effects. The empty space surrounding the sensor represents the p-substrate.