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Analysis and design of an isolated single-phase power factor corrector with a fast regulation

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ABSTRACT

This paper presents an analysis and a modeling approach to obtain a small-signal model design and the digital implementation of a linear control technique for single-phase boost power factor correctors (PFC). Such converters present nonlinear characteristics and approximations of them are used to drive the models. The proposed circuit significantly improves the dynamic response of the converter to load steps without the need of a high crossover frequency of the voltage loop by adding low-pass filter. So, a low distortion of the input current is easily achieved. This controller has been verified via simulation in Simulink using a continuous time plant model and a discrete time controller. Real-time implementation is performed on an experimental test bench utilizing a rapid prototyping tool. The controller is experimentally confirmed for steady-state performance and transient response.

1. Introduction

Single-phase power factor correction (PFC) circuits provide rectification of the line voltage to a regulated dc voltage while shaping the input current to be a sinusoid and in phase with the line voltage [1]. Often, the PFC acts as a pre-regulator to a DC–DC converter that may be used to provide additional regulation and ohmic isolation [2,3]. Due to the adoption of IEC 1000-3-2 [4] as the EN61000-3-2 standard in Europe and the formulation of the IEEE 519 [5] in USA, these circuits are increasingly being used in the front-end of electronic equipments. Among the several possible topologies [2], the boost PFC shown in Fig. 1 is most commonly used. The control objectives are to track the inductor current to a rectified sinusoid (so, the line current is sinusoidal and in phase with the line voltage), to regulate the average output voltage to a desired magnitude and to have a fast response to the load variation [6,7].

Commonly, a linear controller is designed utilizing a small-signal model that is obtained by linearization about an operating point [6]. The system provides acceptable performance. However, the controller has an inherent drawback of third harmonic in the input current. This happens because the reference current signal is the product of an output voltage error amplifier (that contains a second-harmonic component) and the input voltage wave shape. Thus, the voltage loop gain at 100 Hz effectively determines the level of third harmonic to be expected in the input voltage [8]. Several commercial ICs incorporate the required analog components to implement the linear control scheme. Recently, there has been a significant interest in all-digital implementations available for the PFC application; the digital implementation of the linear control design using commercial microcontrollers and DSPs has been carried out. Since the computation time of commercial low-cost microcontroller is significantly high, a discrete version of the conventional analog design cannot be directly implemented without significant modification of the voltage control loop design. To improve the dynamic response of the converter to load steps, the 100 Hz notch filter is inserted to the voltage control loop. The notch filter reduces the amount of second harmonic (to cancel the output voltage ripple) that is reaching the multiplier. Thus, the voltage loop bandwidth can be increased, which leads to a faster transient response, without the penalty of increased third harmonic in steady state. For faster dynamic response, current mode control is adopted instead of voltage mode control. Both peak current mode and average current mode controls are widely used [9]. The main difference between the two methods is that, in the latter, the sensed inductor current signal is averaged and compensated by a current compensation network [10], while in the former; only inductor current is sensed and used [11,12]. Although noise in average current mode control can be suppressed, the architecture of the system with average current mode control is complicated. Therefore, peak current mode control is used, and an optimal proportional integral (PI) controller designed by using a small-signal model is adopted to achieve fast dynamic response, simplicity, and easy implementation. This paper presents a systematic analysis,

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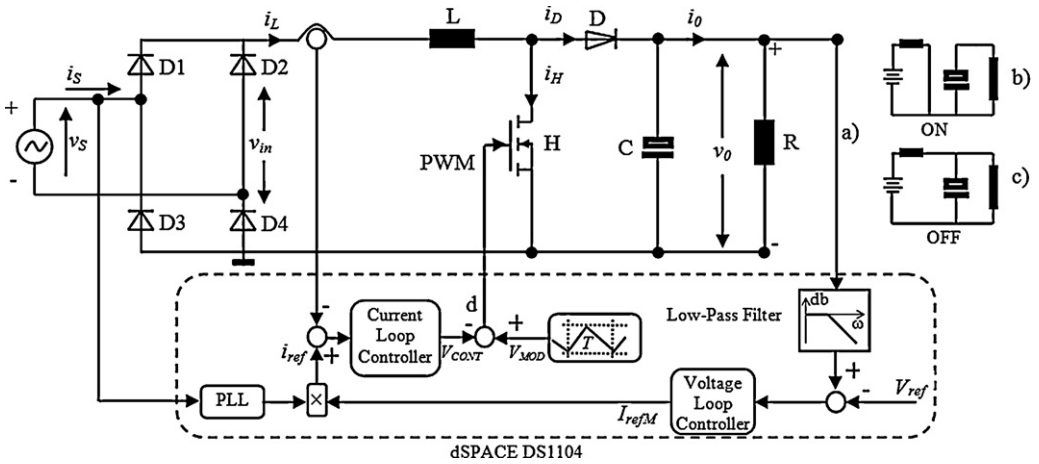

Fig. 1. PFC pre-regulator.

a modeling approach to obtain a small-signal model, design and digital implementation of the standard cascaded linear controller along with using a 100 Hz notch filter in the voltage loop of a regulated dc voltage. This controller is verified by detailed MATLAB/Simulink based on simulations through the use of a continuous time plant model and a discrete time controller. Design is comprehensive in the sense that it accounts for sampling effects, computation delays, hardware filtering for antialiasing, and software filtering for measurement noise reduction, where necessary. Real-time implementation is done on an experimental prototype using the dSPACE DS1104 controller board. This controller is experimentally compared for steady-state performance and transient response over the entire range of input and load conditions for which the system is designed. The paper is organized as follows. In Sections 2–4, we describe the circuit description, the static analysis of power factor corrector and a design example. The design and the analysis for controllers are presented in Sections 5 and 6. Sections 7 and 8 present the details of the simulations and experimental setup with discussions of results.

2. Circuit description

The basic circuit diagram of the DC–DC converter with front end solid state input power factor conditioner used in the proposed scheme is shown in Figs. 1a and 2.

The power circuit is that of an elementary step-up converter. When the boost switch H is turned on ($d=1$) Fig. 1b, the inductor current builds up, and energy is stored in the magnetic field of the inductor, whereas the boost diode D is reverse biased, and the capacitor supplies power to the load. This is the first mode operation. As soon as the boost switch is turned off ($d=0$) Fig. 1c, the power circuit changes mode, and the stored energy in the inductor, together with the energy coming from the input ac source, is pumped to the output circuitry (capacitor–load combination). This is mode 2 of the circuit. Then the state space model for the boost PFC in continuous current mode can be found by the circuit analysis of Fig. 1a. The output voltage and inductor current dynamics are governed by the variable structure real switched system Eq. (1).

$$\begin{cases} \dfrac{dv_0}{dt} = \dfrac{1}{C}\left[(1-d)i_L - \left(\dfrac{1}{R}\right)v_0\right] \\ \dfrac{di_L}{dt} = \dfrac{1}{L}\left[v_{in} - \left(\dfrac{1}{d}\right)v_0\right] \end{cases} \tag{1}$$

In order to obtain a sinusoidal input current in phase with the input voltage, the control unit should act in such a way that v_{in} sees a resistive load equal to the ratio of v_{in} and i_L. This has been done by comparing the actual current passing through the inductor with a current reference, which is derived from v_{in} and have amplitude determined by the output voltage controller.

Since the break frequency of the output filter is very low, one can say that the output voltage is controlled only by the average value of the on-duty ratio of the switch in half cycle of the ac input voltage α:

$$V_0 = \frac{V_{in,ave}}{1-\alpha} = \frac{2}{\pi}V_{SM}\frac{1}{1-\alpha} \tag{2}$$

where d is the logical variable to represent the state of the boost switch, $V_{in,ave}$ is the average value of the full-wave rectified sinusoidal input voltage V_{SM} is the peak value of the sinusoidal input voltage.

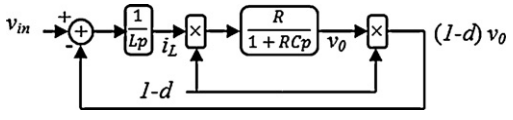

Fig. 2. Block diagram of the PFC pre-regulator.

3. Static analysis of power factor corrector pre-regulators with fast dynamics

The control by current imposes the average power passed to the load with the ideal PFC pre-regulators.

$$P = \frac{1}{T/2}\int_0^{T/2} |v_S(t)||i_0(t)|dt = \frac{1}{T/2}\int_0^{T/2} |V_{SM}\sin\omega t||I_{refDC}\sin\omega t|dt = \frac{V_{SM}I_{refDC}}{2} \tag{3}$$

This behavior in generator of power lets free the voltage v_S to progress according the load R in the ratio v_S^2/R. Generally, the users ask for generators of voltage. It follows the necessity of an automatic adaptation of the power supplied to the load according to its variations to maintain v_S. Fig. 1a shows the voltage loop v_S of which the gating control signal will act on the amplitude of the reference current with a constraint of sinusoidal shape.

Fig. 3 presents a low-pass filter, which is used to eliminate 100 Hz output voltage ripple; I_{refDC} is the peak value of the input