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Small-signal analysis and controller design for an isolated zeta converter with high power factor correction

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Abstract

This paper presents the small-signal model of a proposed isolated zeta converter operating in discontinuous conduction mode (DCM). Based on the derived model, a classical controller is thus designed to tightly regulate the output voltage despite variations in the line voltage and load resistance. The experimental results validate the dynamics and performances of the proposed model. Moreover, the loss-free resistor (LFR) model is applied to verify that the isolated zeta converter exhibits a unity power factor. The operating principle and design considerations are also presented in this work. For the rectifier applications, a low total harmonic distortion (THD) of 9% in the input line current is also obtained. It meets the harmonic regulations of IEC 1000-3-2 Class D standards.

Keywords: Loss-free resistor model; High power factor correction; Isolated zeta converter; Small-signal model

1. Introduction

A rectifier consisting of a diode bridge and a filter capacitor is usually used as a dc voltage supply. However, it causes an impulsive current with a high harmonic distortion and thus the power factor is degraded. A converter is thereby added between the rectifier and the dc/dc conversion stages to achieve high power factor correction (HPFC). To this end, some power converters are operating in discontinuous conduction mode (DCM) to exhibit a HPFC capability [1–10].

In this paper, a zeta power converter is modified into an isolated converter with a grounded switch for electrical isolation and switch driving. The magnetizing inductance L_m and the output inductance L_o satisfy $L_m > L_o$, $L_m < L_o$, or $L_m \ll L_o$. Only the first case, $L_m > L_o$, is considered herein. The loss-free resistor (LFR) model is applied to verify that an isolated zeta converter operating in DCM with $L_m > L_o$ exhibits a unity power factor [11–15]. The cases $L_m < L_o$ and $L_m \ll L_o$ can be analyzed in the same manner presented herein. They also have unity power factor.

According to the operating principle and steady-state analysis, the small-signal model of the proposed isolated zeta converter, operating in DCM with $L_m > L_o$, is then derived by the current injected equivalent circuit approach (CIECA) [16]. The design considerations are also presented in this work. The experimental measurements confirm the dynamics of the proposed model. Based on the proposed model, a PI controller is designed to fast regulate the dc output voltage despite the variations in line voltage and the load resistance.

The PFC capability of the isolated zeta converter and the performances of the closed-loop system are validated by the simulations and experimental results. Additionally, the measured input line current meets harmonic regulations and standards, such as IEC 1000-3-2 Class D. The dependences of the power factor (PF) and total harmonic distortion (THD) on the output power are also presented in this work.

2. PFC capability

The loss-free resistor (LFR) was proposed by Singer in 1990. It is often applied to describe an averaged large-signal

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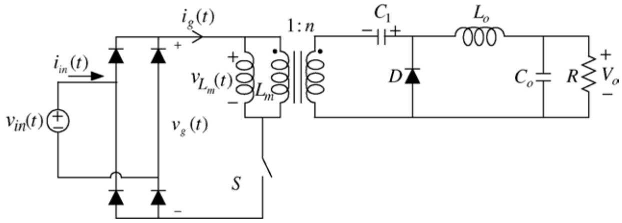

Fig. 1. Isolated zeta converter.

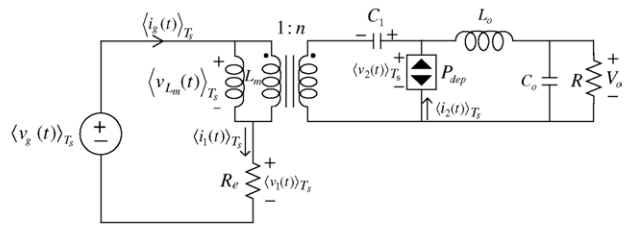

Fig. 2. Loss-free resistor model of the isolated zeta converter.

model of the DCM lossless switch network. In the model, the power switch and the diode can be, respectively, replaced with an emulated resistor R_e and a power dependent source P_{dep}. The power apparently consumed by R_e is completely transferred to P_{dep}. Based on the LFR model, the voltage conversion ratio in the steady state can be easily determined. Moreover, by introducing the small perturbations into the LFR model, the small-signal model of a power converter can also be derived for dynamics analysis.

In addition, the loss-free resistor (LFR) model is powerful for analyzing the power factor correction (PFC) of the converters. If the input impedance is purely resistive in one switching period T_s, then the converter has a unity power factor.

As depicted in Fig. 1, an isolated zeta converter comprises a diode bridge, an isolation transformer, a switch S, an intermediate capacitor C_1, a freewheeling diode D, an output lowpass filter of L_o and C_o, and a load resistance R. The shunt inductor L_m represents the magnetizing inductance of the transformer. Fig. 2 presents the LFR model of the isolated zeta converter. An effective resistance R_e and a dependent power source P_{dep} can be used to replace the switch and the diode of the converter, respectively. In the steady state, the average inductor voltage $\langle v_{L_m}(t)\rangle_{T_s}$ is zero over a switching period T_s because of the principle of the inductor volt-second balance. The magnetizing inductor L_m in Fig. 2 thus becomes a short-circuit and the input impedance is identical to the pure resistance R_e. Hence, the proposed converter has a unity power factor.

3. Operating principle

The analysis of the circuit is based on some assumptions regarding the isolated zeta converter.

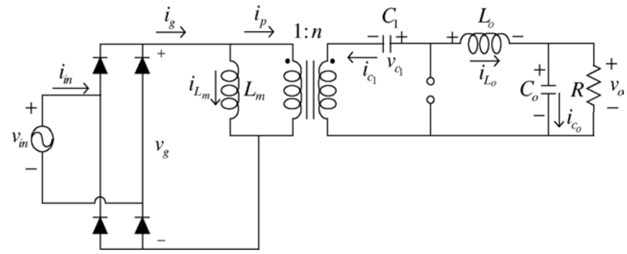

Fig. 3. Equivalent circuit in stage 1.

(a) The rectified line voltage $v_g(t) = |v_m \sin(\omega_L t)|$ is constant during the switching period T_s, where ω_L is the line angular frequency. This assumption is made based on the fact that the switching period T_s is much smaller than the half line period T_L.
(b) The intermediate capacitance C_1 and output capacitance C_o are sufficiently large to be approximated by a constant voltage source.
(c) The inductors and the capacitors of the converter are considered to be ideal without any parasitic components.

Based on the switching of the switch and diodes, the circuit operation of the isolated zeta converter in Fig. 1 can be divided into three linear stages over one switching period T_s. It is operating in DCM with $L_m > L_o$.

Stage 1 $[0, d_1T_s]$ (S: on, D: off): as shown in Fig. 3, the switch S is turned on and the diode D is turned off in this stage. The rectified line voltage v_g is applied directly to the magnetizing inductor and its current i_{L_m} rises linearly. The output inductor current i_{L_o} also rises linearly because the positive voltage $(nv_g + v_{C_1} - v_o)$ is across the inductor L_o. The rectified line current is $i_g = i_{L_m} + i_P$ in this stage.
Stage 2 $[d_1T_s\ (d_1 + d_2)T_s]$ (S: off, D: on): in this stage, the switch S is turned off and the diode D becomes forward-biased. The equivalent circuit is depicted in Fig. 4. Since a negative reflected capacitor voltage $-v_{C_1}/n$ is across the magnetizing inductor, its current i_{L_m} falls linearly. The output inductor current i_{L_o} also falls linearly because of a negative terminal voltage $-v_o$. In this stage, the diode current i_D is $(i_{L_m}/n) + i_{L_o}$.
Stage 3 $[(d_1 + d_2)T_s, T_s]$ (S: off, D: off): in stage 2, the switch S remained off and the inductor currents i_{L_o} and i_{L_m} continue to fall linearly. The diode current i_D also falls linearly because $i_D = (i_{L_m}/n) + i_{L_o}$. When it falls to zero, diode D

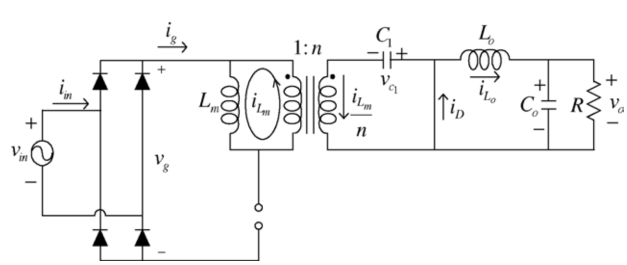

Fig. 4. Equivalent circuit in stage 2.