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Modeling and simulation of a new Bridgeless SEPIC power factor correction circuit

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ABSTRACT

A new Bridgeless PFC circuit based on Single-Ended Primary Inductance Converter (SEPIC) is proposed in this paper. The new topology has less component count and less conducted component during each mode of operation within one switching period. The small-signal and steady-state model of the circuit operated in Discontinuous Conduction Mode (DCM) is derived using the Current Injected Equivalent Circuit Approach (CIECA). The large-signal model based on state-space and switch model are also developed to verify the large-signal behavior. The simulation results of the proposed converter show that the output voltage of the proposed converter is successfully regulated to its desired value while the input current regulation is inherent.

1. Introduction

Power Factor Correction (PFC) circuits are usually comprised of an AC to DC converter with the capability to improve the power factor at the mains. Normally, the PFC circuit is performed by means of a bridge rectifier circuit and a DC–DC converter but some circuit performs this solution without the full-bridge rectifier circuit. This kind of circuit topology is known as the Bridgeless PFC circuit which proposed by Mitchell [1] in 1983 based on the conventional Boost PFC circuit. As shown in Fig. 1a, the Bridgeless PFC circuit consists of two MOSFETs; M1 and M2, two diodes; D1 and D2, an input inductor; L, and output capacitor; C. On the other hand, Fig. 1b shows the circuit topology for the conventional Boost PFC circuit which consist of a full-bridge rectifier and a Boost DC–DC converter. It is obvious that the Bridgeless topology is developed by replacing the lower-part diode rectifier circuit in the conventional Boost PFC circuit with two MOSFETs. As a result, the MOSFET and the output diode in the Boost converter can be eliminated, while the Boost inductor is relocated at the input side.

In the Bridgeless PFC, both MOSFETs are sharing the same control signal and the detail operation of this converter can be obtained in [1]. The Bridgeless PFC circuit is also known as dual-Boost converter due to the similarity of its equivalent circuit with the DC–DC Boost converter during positive and negative half-line cycle. It is found that the number of diodes in Bridgeless PFC (i.e. during ON and OFF state) is less compared to the conventional Boost PFC topology, thus would result in lower conduction losses and hence giving higher efficiency to the whole circuit. Several modifications to this topology have been performed in order to improve the performance of the Bridgeless topology such as reducing the common-mode noise existing in conventional bridgeless PFC [2–5]. Thus, due to the above mentioned characteristics, the Bridgeless PFC circuit is a good candidate for a high-efficiency converter. Beside the bridgeless Boost converter, it is found that other types of converter topologies can also be used to perform the bridgeless PFC such as SEPIC [6,11], Buck [7] and Half-Bridge [8] converter. Among these three topologies, only the SEPIC topology has an inductor at the input side, similar to Boost topology, which is the main

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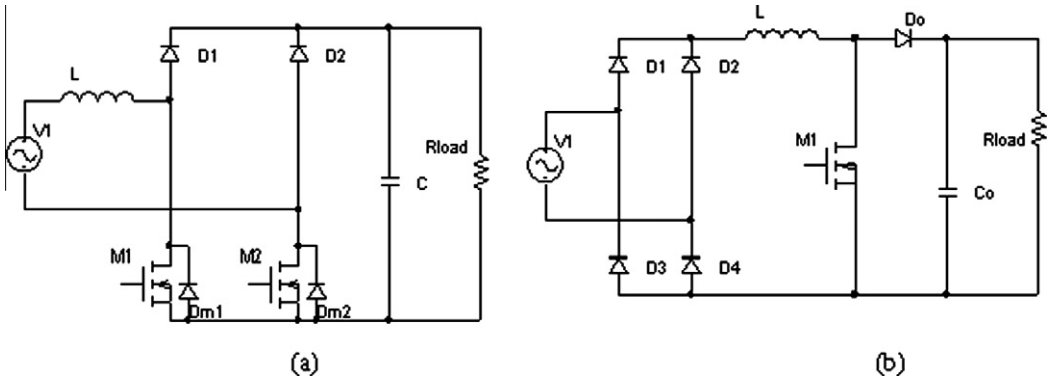

Fig. 1. Schematic diagram of (a) the Bridgeless PFC circuit and (b) the conventional Boost PFC circuit.

factor to obtain high power factor and low current distortion. As reported by Texas Instruments [9], it is found that the performance of SEPIC converter surpasses the Flyback converter in several key issues such as the overall circuit efficiency, switching stress and capability to operate in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). In DCM, the SEPIC converter has two significant advantages as PFC circuits [10] which are: (a) input current will naturally follow the input voltage, thus no current loop is required and (b) isolation can be achieved easily through the second inductor.

Recently, a new Bridgeless PFC based on SEPIC converter has been proposed in [11]. This topology is a combination of two DC–DC SEPIC converters to operate as a single-phase single-stage PFC circuit without input bridge rectifier. The two MOSFETs can be triggered using the same control signal and thus, it is classified as a single-stage converter [12]. However, a gate-drive circuit with transformer isolation is required to drive the two MOSFETs due to its high-side driving characteristics. In addition, two output capacitors at two different terminals are required to filter out the output voltage ripple. As a result, the resistive load is floating which means that both output terminals are not referred to a common ground node of the converter. This feature at the output terminal is not preferred for most application. It is also found that the number of components conducted at each half-line cycle is eleven which is considered high.

In this paper, a new Single-phase Single-stage Bridgeless PFC based on SEPIC converter is proposed. The proposed converter is simpler compared to the Bridgeless SEPIC PFC circuit proposed in [11] while improving several key aspects such as: (a) only one output capacitor is required and the resistive load is not floating, (b) driving the MOSFETs gate terminal is simpler due to low-side driver capability in which a gate-drive with transformer is not required, and (c) less number of components operated at each half-line cycle of input voltage. First, the subinterval modes of the proposed converter are identified with the aid of equivalent circuit and voltage/current waveforms. Then, based on these two results, the small-signal model is developed using Current Injected Equivalent Circuit Approach (CIECA) [14,15] in order to design the closed-loop Proportional–Integral (PI) controller. At the same time, PLECS/Matlab is used to verify the small-signal model obtained from CIECA method. Finally, large-signal switch models based on state-space equations are developed using MATLAB/Simulink and SABER simulator to verify the large-signal behavior.

2. Operating principles of the proposed Bridgeless PFC converter

The proposed Bridgeless PFC circuit diagram is depicted in Fig. 2a. The equivalent circuit during positive and negative half-line cycle is shown in Fig. 2b and c respectively. At positive half-line cycle, all components will conduct except Ds1, S2, C2, L3 and Do2, while at negative half-line cycle Ds2, S1, C1, L2 and Do1 will not conduct. Accumulatively, only eight components will be conducted at each half-line cycle compared to eleven in the bridgeless SEPIC converter proposed in [11]. From this point of view, the proposed circuit will have greater possibilities to perform better in terms of efficiency due to less conducted components.

Although two sets of circuit exist for a complete input voltage cycle, analysis will be carried out only for its positive half-line cycle due to the fact that the same analysis can be carried out during the negative half-line cycle. For high-frequency model, it is assumed that the input voltage is constant within each switching period although it is a well known fact that the magnitude of the sinusoidal input voltage is varied from zero to its peak value and goes back to zero within each half-line cycle. This assumption is made due to the difference between the input mains period and the switching period is very large such that the input voltage seems to be a constant value within each switching period.

However, this assumption will only valid for the high-frequency model which will be derived in the next section. The low-frequency model which is vital in modeling PFC circuit will take into account the sinusoidal wave-shape of the input voltage. On top of that, the analysis will be done with all the inductors operated in DCM. As discussed in [13], the capability of any PFC converter to correct the power factor (i.e. to reshape the input current to sinusoidal and in-phase with the input voltage)