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Overload robust IGBT design for SSCB application

I. Supono [a,*], J. Urresti [a], A. Castellazzi [a], D. Flores [b]

[a] Department of Electrical and Electronic Engineering, University of Nottingham, Nottingham NG7 2RD, UK
[b] Instituto de Microelectrónica de Barcelona, Campus UAB, Cerdanyola del Vallès, Barcelona E-08193, Spain

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ABSTRACT

This paper presents an optimised power semiconductor architecture based on the CIGBT approach to be used in solid-state circuit breaker (SSCB) applications where the conduction losses have to be as low as possible without compromising the forward voltage blocking capability. Indeed, a high overcurrent turn-off and short-circuit withstand capabilities have to be ensured. Starting from a standard NPT-IGBT design for switching applications, the results show that the proposed device, which is optimised by the application of the individual clustered concept, offers a reduction in conduction losses of 13%, without compromise on voltage blocking capability. An original design solution is implemented to further ensure short-circuit and overload turn-off capabilities at maximum ambient temperature and twice the nominal rated current.

1. Introduction

Fault detection and prompt removal is a critical enabler for the development of advanced electrical power transmission and distribution systems. Therefore, reliable circuit breakers as protection devices to prevent system damage and ensure reliability are essential. The performance and ratings of traditional electro-mechanical circuit breakers cannot meet the demands of upcoming distribution systems (e.g., Energy Internet [1]) (Fig. 1). Hence, circuit breakers based on solid-state technology (SSCB) are a promising alternative, as they can bring along several advantages compared to traditional electro-mechanical solutions, such as improved voltage quality during short circuit and reduced short circuit current levels [2–5].

Presently, commercially available IGCTs are the best power devices for SSCB applications. However, SSCB oriented high voltage IGBTs [6–7] would be extremely attractive as they offer many advantages (Table 1) such as reduced switching losses, simpler and more efficient gate driver, competitive price and mature process technology. Particularly for non-punch-through IGBTs the thermal stability is another attractive feature. This paper presents the design and optimisation of bespoke 3.3 kV IGBTs for SSCB applications, based on numerical 2D electro-thermal TCAD simulations and addresses fabrication aspects of optimised final architecture.

2. SSCB bespoke optimisation

The typical situation in SSCB applications is for the IGBT to be in the on-state most of the time. The IGBT is turned-off when faults or overloads happen in the system. So, the reduction of the conduction losses is the key parameter during the optimisation phase of a bespoke power semiconductor device. Assuming that many power devices need to be connected in series to meet the typical voltage levels of transmission and even distribution networks (Fig. 2), it is important that optimisation of the on-state performance does not degrade the blocking capability of the device which would require a higher number of series connected switches (e.g. an 11 kV network needs at least four 3.3 kV IGBTs or seven 1.7 kV IGBTs).

Taking into account the SSCB requirements, the most important features when optimising a power semiconductor device are the maximum overload (current and temperature) turn-off capability, as well as the short circuit withstand capability. The robust handling capability against the two situations is essential for devices in SSCB because overload caused by excessive electric consumption and overcurrent caused by short circuit are fault conditions that likely occur in power transmission/distribution lines.

The IGBT optimisation starts from a selected reference device with an NPT-planar architecture (core cross-section plotted in Fig. 3a), typically designed for switching applications and rated at 3.3 kV–100 A. The device high voltage drop (indicated by 4.25 V at 50 A/cm^2) hints the possibility of device conduction losses improvement. The device is fabricated on a 500 μm thick wafer with a doping profile shown in Fig. 3b. A new proposed structure is inspired by the clustered IGBT (CIGBT) concept, schematically illustrated in Fig. 4, which is promoted in reducing conduction losses with a simple application of two additional deep diffusions [8–11]. Regarding these additional layers there are four

* Corresponding author.

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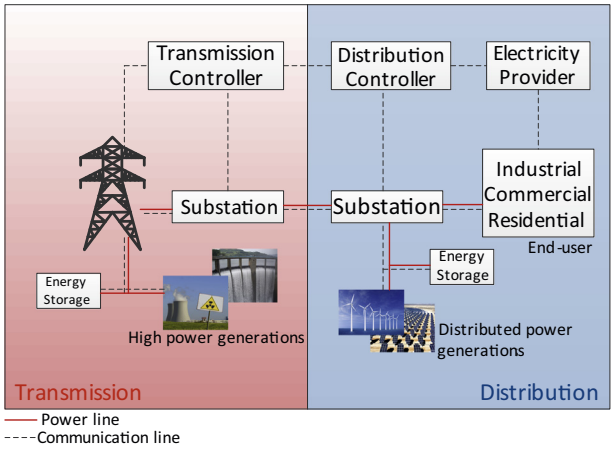

Fig. 1. Smart grid power distribution system.

Table 1
Summary of benchmark performance comparison of the different power device.

Feature	IGBT	GTO	IGCT
Conduction losses	High	Low	Low
Switching losses	Low	High	Medium
Failure mode	Open/short circuit	Short circuit	Short circuit
Gate driver	Simple, compact	Complex, separated	Complex, integrated
Gate driver power consumption	Low	High	Medium

optimisation parameters: doping concentration and thickness of the two new layers.

The doping profile of the proposed architecture is shown in Fig. 4b including the tuning parameters. Two approaches have been considered, depending on the thickness of the P-base layer. The first case is based on a narrow P-base layer where the P-base junction ($J_{P.base}$) is set at 2 μm (opt-1 case), while the second case (opt-2 case) is contemplates the use of the same P-body characteristics as those of the reference IGBT (7 μm junction depth). The optimisation of the four relevant parameters is divided into two groups, depending on the final target. The concentration and thickness of the additional P-layer ($C_{Add.P}$ and $t_{Add.P}$) are optimised to sustain the required breakdown voltage while the additional N-layer ($C_{Add.N}$ and $t_{Add.N}$) is optimised to get the minimum conduction losses. The starting point and the optimisation methodology are depicted in Fig. 5.

The global target for the proposed architecture is to obtain the minimum conduction losses at 50 A/cm^2 current density while maintaining the 3.3 kV blocking capability. In order to be able to detect a fault event with the subsequent safe turn-of of the SSCB, two constraint parameters are set: the 100 A/cm^2 overcurrent and the 10 μs short circuit withstand capabilities, both at an ambient temperature (T_{AMB}) of 125 °C.

The IGBT and the proposed structures are implemented and simulated with Silvaco™Atlas® [12]. Isothermal conditions are used for the steady-state analysis (on-state vs. blocking voltage performance), while fully coupled mixedmode electrothermal simulations are performed for the transient analysis (turn-off and short-circuit capability). The self-heating effect model includes an estimated 4 cm^2 K/kW thermal resistance between the collector electrode (device backside) and the thermal ground (ambient temperature of 125 °C).

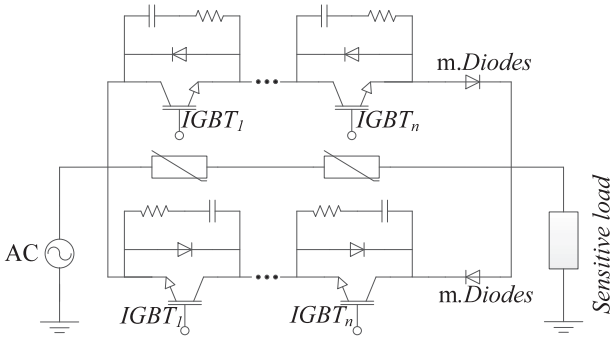

Fig. 2. Schematic circuit of SSCB for ac based on IGBTs and diodes.

3. Simulation results and design optimisation

The optimised additional P-layer for the opt-1 case corresponds to a maximum doping concentration ($C_{add.N}$) of 3×10^{15} cm^{-3} and

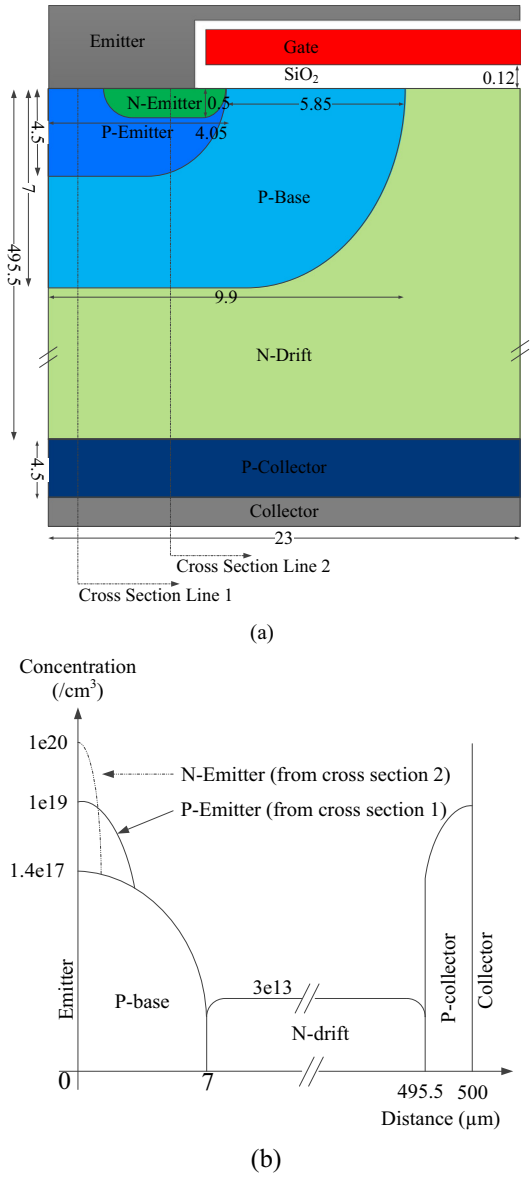

Fig. 3. Reference 3.3 kV IGBT structure. Core cross-section (a) and doping profile (b).