Applied Soft Computing 38 (2016) 955–966

Contents lists available at ScienceDirect

Applied Soft Computing

journal homepage: www.elsevier.com/locate/asoc

# A hybrid evolutionary algorithm for multiobjective variation tolerant logic mapping on nanoscale crossbar architectures

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ARTICLE INFO

*Article history:*
Received 13 January 2015
Received in revised form 22 October 2015
Accepted 24 October 2015
Available online 1 November 2015

*Keywords:*
Nanoscale crossbar
Variation tolerant logic mapping
Bilevel multiobjective optimization
Hungarian-based linear programming
Hybrid evolutionary algorithm

ABSTRACT

Nanoscale crossbar architectures have received steadily growing interests as a result of their great potential to be main building blocks in nanoelectronic circuits. However, due to the extremely small size of nanodevices and the bottom-up self-assembly nanofabrication process, considerable process variation will be an inherent vice for crossbar nanoarchitectures. In this paper, the variation tolerant logical mapping problem is treated as a bilevel multiobjective optimization problem. Since variation mapping is an NP-complete problem, a hybrid multiobjective evolutionary algorithm is designed to solve the problem adhering to a bilevel optimization framework. The lower level optimization problem, most frequently tackled, is modeled as the min–max-weight and min-weight-gap bipartite matching (MMBM) problem, and a Hungarian-based linear programming (HLP) method is proposed to solve MMBM in polynomial time. The upper level optimization problem is solved by evolutionary multiobjective optimization algorithms, where a greedy reassignment local search operator, capable of exploiting the domain knowledge and information from problem instances, is introduced to improve the efficiency of the algorithm. The numerical experiment results show the effectiveness and efficiency of proposed techniques for the variation tolerant logical mapping problem.



## 1. Introduction

Although the complementary metal oxide semiconductor (CMOS) technologies have met the demand of increasing functionalities by scaling exponentially as Moore's law predicted in the past four decades, the scaling is predicted to approach fundamental limits at the end of next decade [1]. Nanoelectronic technologies (circuits built with components on the scale of 10 nm) [2] has recently been studied as one possible heir to CMOS technologies to continue the scaling when CMOS technologies hit their limit. Some novel nanoelectronic devices have been fabricated and characterized in chemistry labs using bottom-up approach (in which devices are created by chemical assembly instead of top–down–based lithography) [3], such as carbon nanotube field-effect transistors (CNT-FETs) [4], nanowire field-effect transistors (NW-FETs) [5], and single electron tunneling junctions (SETJs) [6]. Using nanoelectronic devices and bottom-up approach could achieve more scaling and make it possible to produce higher speed, higher density, and lower power consumption electronic systems compared to customer CMOS technologies.

However, variations caused by the nanoelectronic technologies are expected to be much more serious than the CMOS technologies. At the nanoscale level, even an uncertainty of a few atoms may adversely affect the parameters and the behavior of nanoelectronic devices. There are various sources of variations for the new technologies: variations in the features of nanowires and nanotubes caused by stochastic assembly process [7,8], material density variations resulted from the lack of precise control over material positioning [9,10], and variation of resistance due to poor connections of crosspoints [8,11]. Such variations might prevent circuits from meeting timing and power constraints and degrade the parametric yield [12]. Therefore, variation tolerant techniques will be crucial to the generalization of bottom-up nanoelectronics technologies.

Nanoscale crossbar architectures have been widely studied [13–15] for their great potential to be main building blocks in nanoelectronic circuits. They are the easiest computational structure to fabricate at nanoscale and have the merit of configurability, interchangeability, and regularity [16]. Similar to the programmable logic array (PLA) [17], a nanoscale crossbar consists of two layers

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http://dx.doi.org/10.1016/j.asoc.2015.10.053
1568-4946/

of orthogonal nanowires. Variation tolerant logic mapping (VTLM) problem can be defined generally as: given a crossbar and a logic function to be implemented on it, find a mapping of the logic function to the crossbar with consideration of variation of delay. The VTLM is one critical technique to mitigate process delay variation by utilizing the reconfigurable nature of the crossbar. There exist $n! \times m!$ permutations for an $n \times m$ logic mapping problem, so it is intractable for exhaustive methods to deal with large scale crossbars. Some previous works [18–23] have investigated the VTLM in different ways, which can be broadly divided into three types according to the objectives set for optimization.

Ghavami et al.et al. [18] and Zamani et al.et al. [22] considered minimizing the maximum variation as the design objective. In [18] a mathematical model based on weighted bipartite a graph is proposed, after which a greedy algorithm is presented to solve VTLM. The method shows great advantage over exhaustive method in terms of runtime. However, the authors did not pay much attention to the effectiveness, quality of the solution of the algorithm, which depended much upon the nature of the benchmark problems. In [22] a set of interger linear programming (ILP) formulations is introduced to solve the VTLM, and the experimental results show this method can find better results at a higher time cost compared to simulated annealing [19], the computational complexity of the method would be further high if the size of crossbar becomes larger.

Tunc and Tahoori [19,20] took into account two optimization objectives (minimizing maximum delay and minimizing output variations) separately for mapping a function to a crossbar. They translated the logic mapping problem into the mapping between two matrices by exploiting variation matrix (VM) and binary function matrix (FM). A simulated annealing (SA) algorithm was used to optimize the matrix mapping, its effectiveness was testified with better experimental performance over the exhaustive method. With their approach, since the optimizations of the two objectives are conducted separately, optimizing with respect to one objective may result in a bad performance with respect to the other objective.

Very often, a decision maker prefers an approximation of the Pareto front for a good insight to the problem and making his or her final choice. In order to get a set of good (in the sense of Pareto optimum) solutions to be examined for trade-offs rather than a single solution, Yang et al.et al. [21] formulated the VTLM problem into a multiobjective optimization problem, and used an evolutionary algorithm, NSGA-II, to get a set of nondominated solutions. Experimental results show that the obtained solutions are close to the Pareto front of the benchmark problems of small sizes. However, NSGA-II shows its performance degrading when the size of crossbar becomes larger. To improve the performance of NSGA-II, Zhong et al.et al. [23] introduced a greedy local search into NSGA-II and presented a hybrid NSGA-II, which could find better solutions than [21].

To make the VTLM problem more tractable, the problem can be treated as a bilevel multiobjective optimization problem (BLMOP), where the tough problem can be divided into two level of correlated subproblems, and be solved respectively with different methods. Bilevel optimization problems, arise from hierarchical problems in practice, are characterized by the existence of one (lower level) problem embedded in other (upper level) optimization problem. BLMOP involve optimization of multiple objectives at one or both of the levels [24]. Though many works [25,26] have been done for bilevel single-objective optimization, not much attention has been paid to the BLMOP until recent years [27–31]. Deb and Sinha [27] proposed a viable algorithm based on evolutionary multiobjective optimization (EMO) principles to solve BLMOP. Based on those studies, Deb and Sinha [28] proposed a hybrid evolutionary local search-based algorithm as a solution methodology, Sinha [29] presented a progressively interactive EMO for bilevel problems, where preference information from the decision maker at the upper level of the bilevel problem is used to guide the algorithm toward the most preferred solution. Zhang et al.et al. [30] proposed an improved particle swarm optimization (PSO) for solving BLMOP, which was further improved in [31] by hybrid with a crossover operator to prevent premature convergence. These algorithms are able to solve generic bilevel multiobjective optimization problems, but not efficient enough for the VTLM problem.

In this paper, the VTLM problem is treated as a bilevel multiobjective optimization problem and a hybrid multiobjective evolutionary algorithm (HMOEA) is designed to solve the problem in a bilevel optimization framework [28,32]. The lower level optimization problem is modeled as the min–max-weight and min-weight-gap bipartite matching (MMBM) problem, which is defined in weighted bipartite graph as a perfect matching, where both the maximal edge weight and edge weight gap are minimized simultaneously. A Hungarian-based linear programming (HLP) method is proposed, which can solve MMBM in polynomial time. The upper level optimization problem is based on optimality of the lower level optimization problem. An evolutionary multiobjective optimization is designed to solve the upper level optimization problem, where a greedy reassignment local search operator, capable of exploiting the domain knowledge and information from problem instances, is introduced to improve the efficiency of the algorithm. The numerical experiment results show the effectiveness and efficiency of the bilevel optimization framework and the proposed hybrid evolutionary algorithm.

The remainder of this paper is organized as follows. In Section II, the statement of the VTLM problem for nanocrossbar architectures are described. Section III provides the formulation of the optimization problem. Section IV introduces the proposed hybrid optimization algorithms. In Section V, experiment results, comparisons, and analysis are presented. Finally, Section VI concludes the paper.

## 2. Statement of the problem

A nanoelectronic crossbar consists of two series of orthogonal nanoscale wires with configurable devices at the crosspoints (junctions). Each junction can be independently activated or deactivated. If a junction is deactivated, its corresponding crossing wires do not interact electrically. When it is activated, two wires of the junction are connected to behave as a diode or a transistor, depending on the nature of nanowires. Fig. 1 shows an example of general structure of two-dimensional crossbar.

Using the programmable architectures, researchers have presented logic operations implanted on diode-based crossbar and FET-based crossbar [33]. The diode-based crossbar can be used to implement wired OR logic as shown in Fig. 2a. While the FET-based crossbar can not only build NAND logic as shown in Fig. 2b, but also NOT, AND, NOR, and OR logic [33].

The lumped delay information in a crossbar can be represented by a real matrix called variation matrix (VM) [19,21]. Each entry

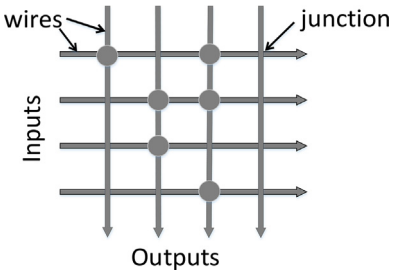


**Fig. 1.** Schematic of the crossbar with configurable junctions. Junctions with dot represent the activated state.