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Implementation of Digital Electronic Arithmetics and its application in image processing

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A R T I C L E I N F O

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A B S T R A C T

In this paper we introduce new algorithm implementations of a new parametric image processing framework that will accurately process images and speed up computation for addition, subtraction, and multiplication. Its potential applications include computer graphics, digital signal processing and other multimedia applications. This Parameterized Digital Electronic Arithmetic (PDEA) model replaces linear operations with non-linear ones. The implementation of a parameterized model is presented. We also present the design of arithmetic circuits including parallel counters, adders and multipliers based in two high performance threshold logic gate implementations that we have developed. We will also explore new microprocessor architectures to take advantage of arithmetic. The experiments executed have shown that the algorithm provides faster and better enhancements from those described in the literature. The FPGA chips used is Spartan 3E from Xilinix. The critical length in the circuit implemented on the FPGA had the minimum period for the proposed subsystem is 10.209 ns (maximum frequency 97.957 MHz). Maximum power consumed is 2.4 mW using 32 nm process and we used parallelism and reuse of the Hardware components to accomplish and speed up the process.

1. Introduction

In recent years, improvements in imaging technology have made available an incredible array of information in image format. Image processing is the system of mathematically transforming an image from one form or another, generally to change some characteristics of the image [1]. The demand for handling images in digital form has increased dramatically in recent years. In order to utilize digital images effectively, specific techniques are needed to reduce the number of bits required for their representations [1]. Different coding techniques have been developed for use in simplifying and optimizing these reductions. From Shannon's Information Theory, we know that for a given information source like an image there is a coding technique which permits a source to be coded with an average code length as close as to the entropy of the source as desired [2]. One of the studies shows squaring to be effective; this approach is commonly used in digital signal processing applications. Significant performance increases can be achieved by supporting squaring circuits in hardware [27].

The demand for handling images in digital form has increased dramatically in recent years. In order to utilize digital images effectively, specific techniques are needed to reduce the number of bits required for their representations [28]. In developing image processing techniques, Stockham has noted that it is of central importance that an image processing framework be physically consistent with the nature of the images, and that the mathematical rules and structures that are employed must be compatible with the information to be processed [8]. Another example is what Granrath recognized

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to be the important role of simulating the mechanisms of human vision when developing models for image processing. He also highlighted the symbiotic relationship between the study of image processing and of the human visual system [9]. In his study of vision, a computational investigation into the Human, Marr has pointed out that, to develop an effective computer vision technique, the following three points must be considered: first, what are the particular operations to be used and why? Second, how will the images be represented, and finally, what implementation structure can be used [10]? Myers has also pointed out that there is no reason to persist with the classical linear operations, if, through abstract analysis, more easily tractable or more physically consistent abstract versions of mathematical operations can be created for image and signal processing [11].

Traditionally, image processing makes use of linear operations to manipulate images, but since this is inherently a non-linear process, accuracy issues can arise. First, when resulting pixel intensities lie outside the range (0, M), they are clipped, causing a loss of information. Second, linear operations typically do not yield results consistent with the physical phenomena (as perceived by human eye/brain). By solving these common problems in an image processing context, the methods can be utilized to improve many other areas of signal processing. Some study as in [29] shows color still images of 512 by 512 pixels that were first converted to the corresponding monochrome images in order to generate their contours using the Sobel filter [29]. Computational approaches have recently engendered a renewed interest in logarithmic image processing and applications. During the last twenty years, successful application examples were reported in a number of image processing areas; for example, background removing [23], illumination correction, image enhancement (dynamic range and sharpness modification), image 3D-reconstruction and visualization, contrast estimation [26,27], image restoration and filtering. In real-time systems, the overall execution time has primary importance and therefore, especially the enhancement algorithm must be fast and effective [30].

In this paper, we presented an optimized implementation of the Parameterized Digital Electronic Arithmetic (PDEA) approach for implementing computer arithmetic. It replaces linear operations with non-linear (logarithmic image processing) ones. We also present the design of arithmetic circuits including parallel counters, adders and multipliers based in two high performance threshold logic gate implementations. This paper is organized as follows: Sections 2 and 3 present's background and the Parameterized Digital Electronic Arithmetic (PDEA) format, benefits (advantages) and limitation (disadvantages). Section 4 presents applications. Section 5 presents assumptions and hardware implementations, and Section 6 presents results and a conclusion.

2. Background: the logarithmic image processing approach

The logarithmic image processing (LIP) approach was originally developed by Jourlin and Pinoli and formally published in the mid-1980s for the representation and processing of images valued in a bounded intensity range [15]. The logarithmic image processing (LIP) model treats images as light absorption filters, as shown in Fig. 1 [4]. The PLIP basic operations are directly defined as follows:

$$g1 \oplus g2 = g1 + g2 - \frac{g1g2}{\gamma(M)} \tag{1}$$

$$g1 \Theta g2 = k(M)\frac{g1 - g2}{K(M) - g2 + \varepsilon} \tag{2}$$

$$g1 \otimes g2 = \varphi^{-1}(\varphi(g1).\varphi(g2)) \tag{3}$$

$$\varphi(g) = \lambda(M).\ln^{B}\left[1 - \frac{g}{\lambda(M)}\right] \tag{4}$$

$$\varphi(g)^{-1} = -\lambda(M) \cdot \left[1 - \exp\left(-\frac{g}{\lambda(M)}\right)^{1/B}\right] \tag{5}$$

where, the parameters $\gamma(M)$, $k(M)$, and $\lambda(M)$ are linear functions of the type, $\gamma(M) = AM + B$; A and B are constant parameters.

3. Proposed Parameterized Digital Electronic Arithmetic

In this section, the proposed serial-parallel architecture for wavelet image compression and decompression is described. We first introduce the notation and the wavelet function used in our system.

Despite the inherent advantages of the LIP model over linear image processing, there are systems in which neither LIP nor linear arithmetic systems will work. Fig. 2 shows a concatenated adder system, which takes an input image and adds it to itself several times. Using linear arithmetic for the adder blocks, the result will be out of range for many images, especially bright images. If linear arithmetic is being performed with an 8-bit per color architecture, this information in the overflow is simply lost. If the LIP model is used, it will not overflow; however, the output image will quickly be driven to saturation [1].