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Analysis and simulation of Single Electron Transistor as an analogue frequency doubler

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ABSTRACT

Performance of Single Electron Transistors as analogue frequency doublers is evaluated by analysis and HSPICE simulations. First, a macro model is selected which represents the device characteristics adequately. The model parameters are determined for different devices reported in the literature, based on their DC characteristics. Adding terminal capacitances to the device model, the small-signal AC performance of the transistors are then simulated. It is observed that the selected devices can operate up to GHz frequencies. Then large signal theory of operation of a common source doubler with resistive loading is developed based on the selected model. Simulations for resistor and transistor loaded circuits with HSPICE are also presented. There is good agreement between the simulation results and those from the closed form analytical expressions. The device analysis and simulations indicate that the device can be used as a doubler in its Coulomb blockade region of operation. Conversion gain (loss) of −13 dB, and harmonic distortion of 12% can be expected.

1. Introduction

Since the early work on understanding fundamentals and potential of Single Electron Transistors [1,2], there have been growing interest in these devices for the past decades [3,4]. On its path of development, the simulation of devices, circuits, and systems have followed the early work.

The evolution of the device has included various modelling efforts. The computationally intensive Monte Carlo models have been introduced by Chen and Washuber [5,6]. The results of the Monte Carlo models often serve as the benchmark for other modelling activities namely, analytical [7–9] and macro models [10–15]. The advanced fabrication technology required for these transistors has limited the number of devices actually built and measured [16]. To the best of our knowledge, there is not enough experimental data to be considered as a typical device performance. Hence, many have relied upon Monte Carlo simulations. Macro models have traditionally been the favourite choice for circuit simulations. We have selected one of the early macro models by Yu et al. [12], for our work. The favourable characteristics of this model are the simplicity, ease of implementation, and satisfactory predictive power.

Digital circuit and eventually sub-system simulations have followed the device work. The circuit simulations have demonstrated logic gates [11,12]. More complex structures such as SET-CNN [17], SET-CMOS hybrid [18], and SET Network on Chip [19], have also been demonstrated.

Because of the small size of the SETs, and potential for very high level of integration, the focus of the circuit development has been on digital circuits with limited work on analogue applications [7,20]. In this work, we will analyse and simulate the performance of a SET analogue frequency doubler. Frequency doublers can be used for waveform generation at a higher frequency when building a fundamental oscillator proves difficult. The ability of the SET as a doubler is a natural consequence of its oscillatory drain current versus gate voltage transfer characteristic.

In what follows, we will first use our selected macro model to fit the DC characteristics of three SETs given in the literature. The capacitive elements are added to the circuit model for the simulation of the small-signal frequency response. Then the theory of operation of a common source doubler with resistive loading is presented. Doubler performance parameters such as conversion gain (loss), its dependence on input amplitude and supply voltage, and harmonic distortion as predicted by the theory and simulated by HSPICE is shown. The reasons for discrepancies between the calculated and simulated results are given. Finally, a single-stage common source configuration with transistor loading is considered. Here only results of simulations by HSPICE are presented. In addition to the above performance parameters, the frequency limits of large signal operation will be given for the transistor loaded circuit.

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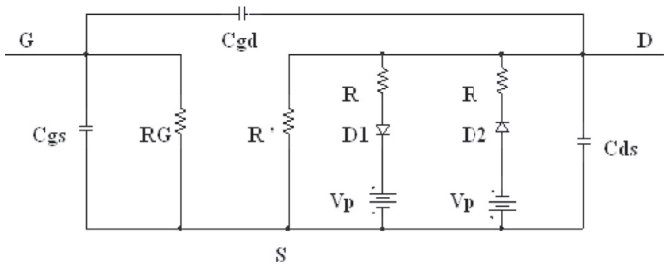

Fig. 1. The equivalent circuit model used for the SET.

2. Device model

The choice of the device model is one of the important factors in circuit simulations. Macro models are traditionally used for circuit simulations, because of their computational efficiency. We have selected one of the early macro models for our circuit simulations, namely the model developed by Yu [12]. By appropriate addition of internal device capacitances we have been able to extend the model to high frequencies. In this section, we first discuss the basic model followed by extension to AC analysis and simulation.

2.1. The macro model

The circuit diagram of the Yu model is shown in Fig. 1, excluding the terminal capacitances. The drain to source part of the circuit model is composed of three branches. The controlled resistor R' represents the Coulomb blockade phenomenon observed in these devices. The other two branches become significant for higher drain source voltages with opposite polarities. The circuit elements are described by the following equations [12].

$$R' = R_1 + R_2 \ \ Cos(\ K \cdot \pi \cdot \ Vgs\ ) \tag{1}$$

$$R = \frac{V_p}{I_p - 2\ \frac{V_p}{R'}} \tag{2}$$

Where R_1, R_2, K, V_p, and I_p are the fitting parameters to be determined. V_{gs} is the gate to source voltage. Equation (1) shows the gate voltage dependence of the circuit element R'. The cosine variation of this resistor results in the oscillatory transfer characteristic. The value of the resistor R in the circuit model is also dependent on R'. For the diodes, we have used the usual equation given below.

$$I = I_s \left[e^{\frac{qV}{kT}} - 1 \right] \tag{3}$$

The parameter definitions are well known.

There have been modifications to this model up to recent years [10,11,15], with the purpose of improvement. Karimian et al. [10] added a quantizer block to account for the tunnelling time. Wu et al. [11] modified the voltage dependence of the resistors to include the effect of the drain to source voltage. The aim was to improve the prediction of the dependence of the drain current on the drain to source voltage. In another attempt to achieve the same goal, Ghosh et al. [15] had to add new circuit components to the original model. However, all of these added to the complexity. We believe the model in its original form captures the key characteristics of the device for the doubler circuit operation. Including the enhancement features of the later authors would make the analytical calculations a formidable task. We have found that it is capable of reasonably accurate prediction of device characteristics for symmetric SETs.

Three devices with their characteristics given in the literature were selected to implement the macro model. These devices were named A [11], B [17], and C [7]. Device A characteristics were obtained with the macro model developed by Wu et al. [11], and their results were examined against the predictions of the Monte Carlo simulator SIMON 2.0. The device A temperature was at 30 K [11]. Their model was a modified version of the Yu model [12]. The DC characteristics for device B were also generated by the simulator SIMON 2.0 working at room temperature 300 K [17]. The macro model was not used in their work. The characteristics for device C were given in the paper by Mahapatra et al. [7]. Their characteristics were generated using their analytical model incorporating physical events. Their model was also tested against SIMON. They did not use a macro model either, and their operating temperature was 15 K.

Table 1
Summary of model parameters for the three selected devices.

Parameter	Device A	Device B	Device C
R_G (Gohm)	100	100	100
T (K)	30	300	15
K (1/V)	40	3.75	25
R_1 (Mohm)	1600	120	15
R_2 (Mohm)	850	100	10
I_p(nA)	0.075	2.5	8.5
V_p (mV)	20	20	14
I_s (pA)	20	0.1	1E-5
C_g (aF)	3.2	0.3	2
C_d (aF)	1.6	0.1	1
C_s (aF)	1.6	0.1	1
C_{gs}(aF)	0.8	0.06	0.5
C_{ds} (aF)	0.4	0.02	0.25
C_{gd} (aF)	0.8	0.06	0.5

We have replicated the DC characteristics of these devices using the Yu model [12] with the parameters given in Table 1. Fig. 2 (a) shows the drain current versus gate-source voltage for the device A, in the Coulomb blockade region. These plots are in agreement with the characteristics given by Wu et al. in Ref. [11]. To the extent possible, we read some points from the Monte Carlo plots given for the device A. These points are shown by circles in Fig. 2(a). At first glance, the transfer characteristic seems different from the macro model. But a closer look reveals that much better agreement is obtained by a shift of the horizontal axis V_{gs} by 10 mV. The shifted version is shown by the dashed line. The offset in the V_{gs} axis can easily be implemented in the Macro model by insertion of a DC voltage source in series with the gate resistance R_G. The dashed curve in Fig. 2(a) includes the effect of this series voltage source and shows much better agreement with reference data.

The transfer characteristic for the devices B and C are shown in Fig. 2 (b) and (c). Here again, the open circles are those from the references. While the results for the device B agree favourably with those given by Gerousis et al. in Ref. [17], but for the device C [7] we notice a shift of the Vgs values and the agreement can only be considered adequate. Finally, it should be mentioned, to evaluate the model we had to read points from printed documents and we expect some errors to occur.

Despite the shifted characteristics, the macro model prediction of the span of the gate -source voltage and the drain current for all three devices can be considered good. Indeed, these are the important parameters which determine the potential of the SET as a doubler. In the next section, we extend the model for predictions of frequency response.

2.2. The small-signal AC model extension

Considering the macro model for small-signal operation, we have to replace the diodes with their dynamic resistances and the variable resistor with its nominal value at the given applied bias voltage. This results in a purely resistive network with flat small-signal frequency response. Therefore, to obtain the small-signal frequency response of the device we have to add the terminal capacitances.

With the satisfactory evaluation of the DC aspects of the device model, we now use the capacitor values given for these devices [7,11,17], to predict the small-signal AC performance of the SETs. The capacitance values given for the respective devices are repeated in Table 1.